


LCFC Confidential

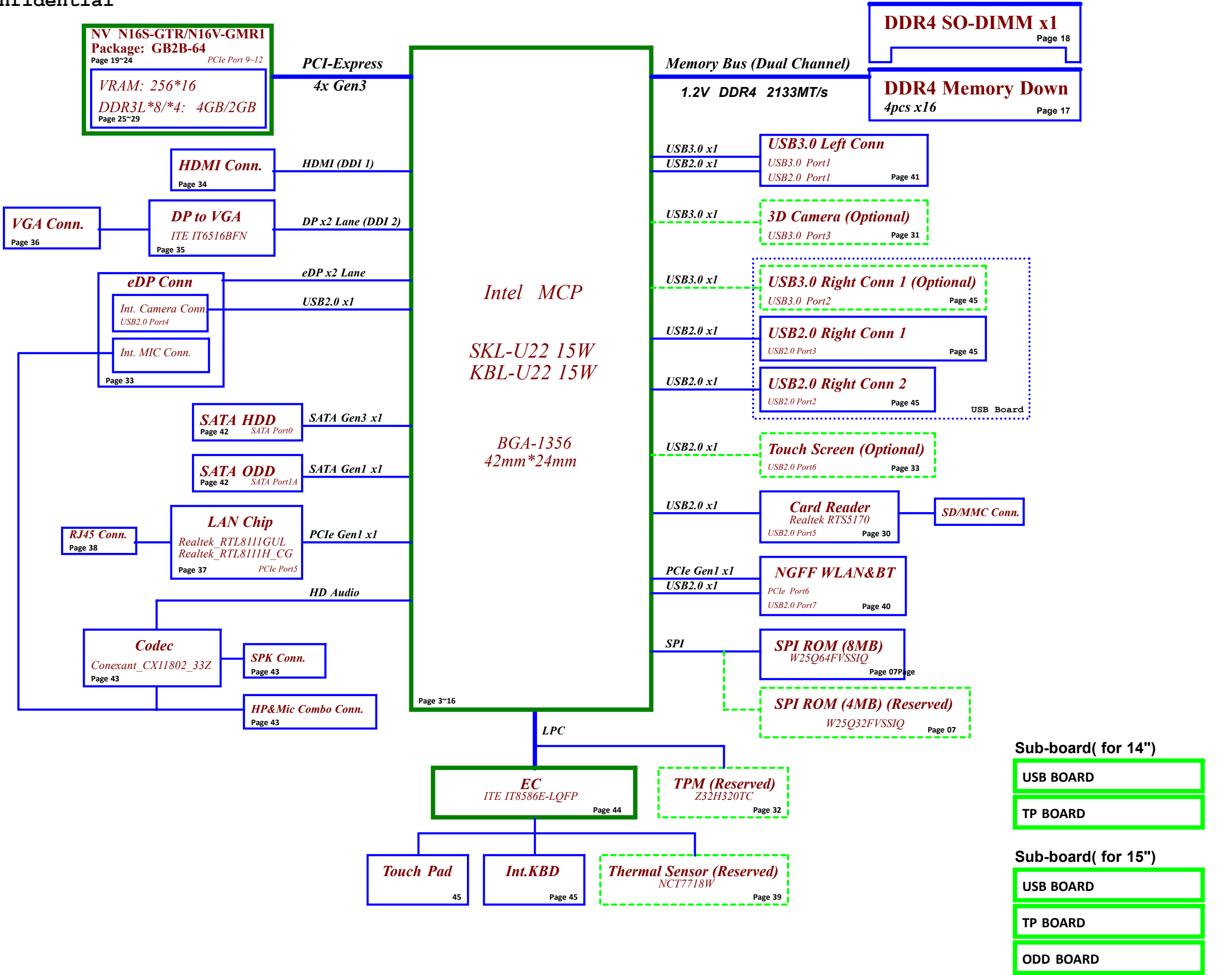
CG411/CG511 MB Schematics Document

Intel Skylake-U22/Kabylake-U22 with DDR4 + Nvidia N16S-GTR/N16V-GMR1 GPU

2016-01-09

REV: 1.0

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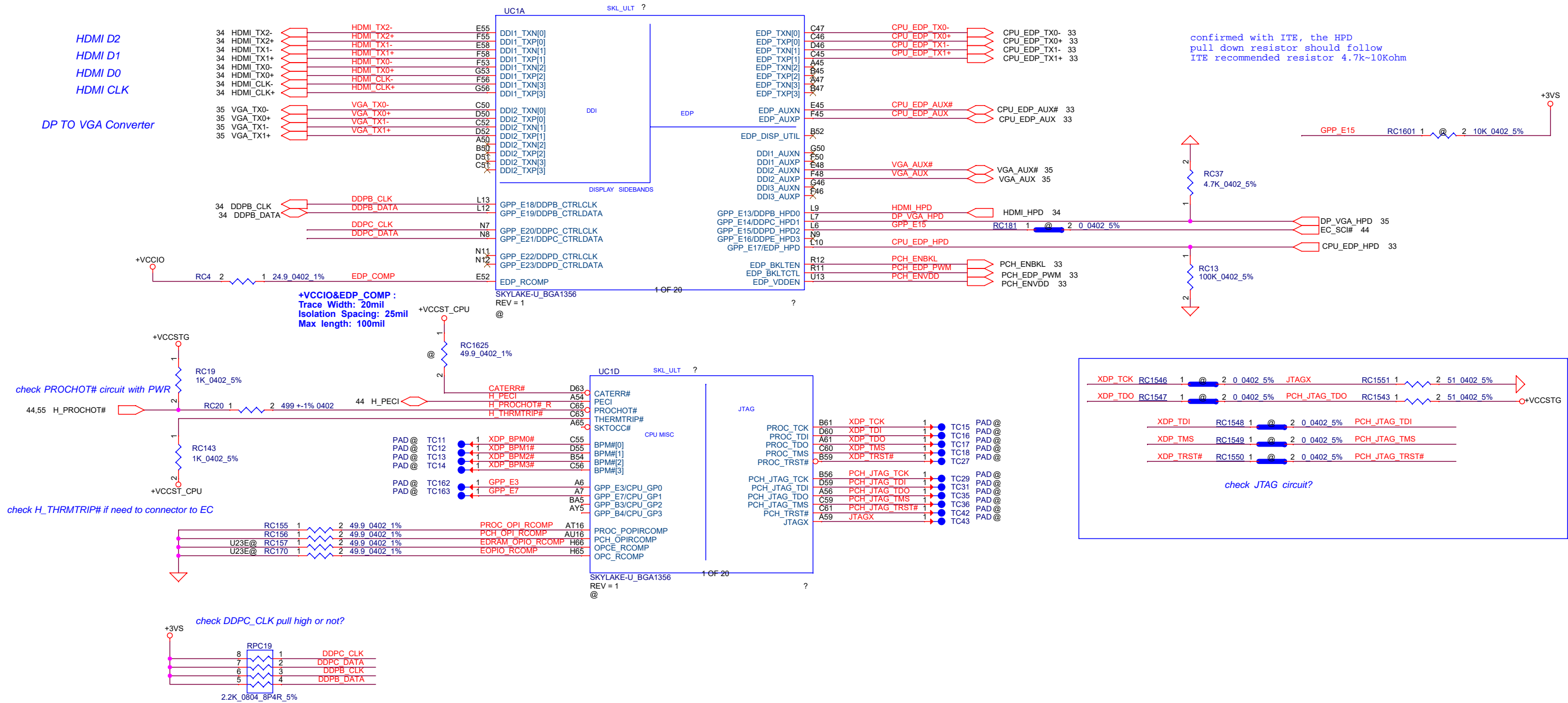


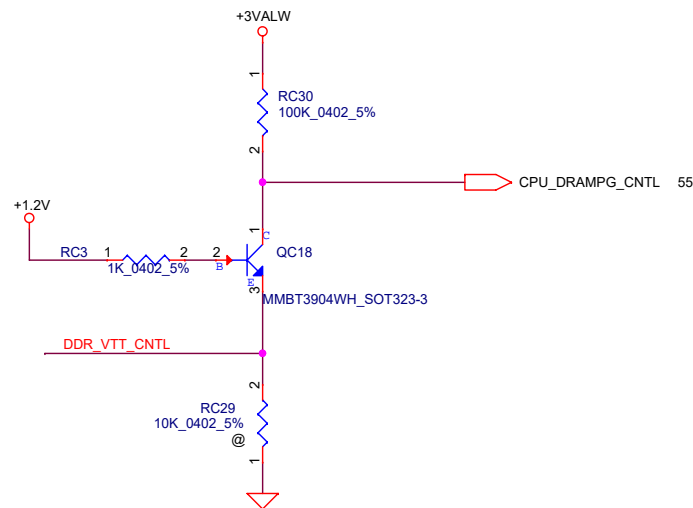
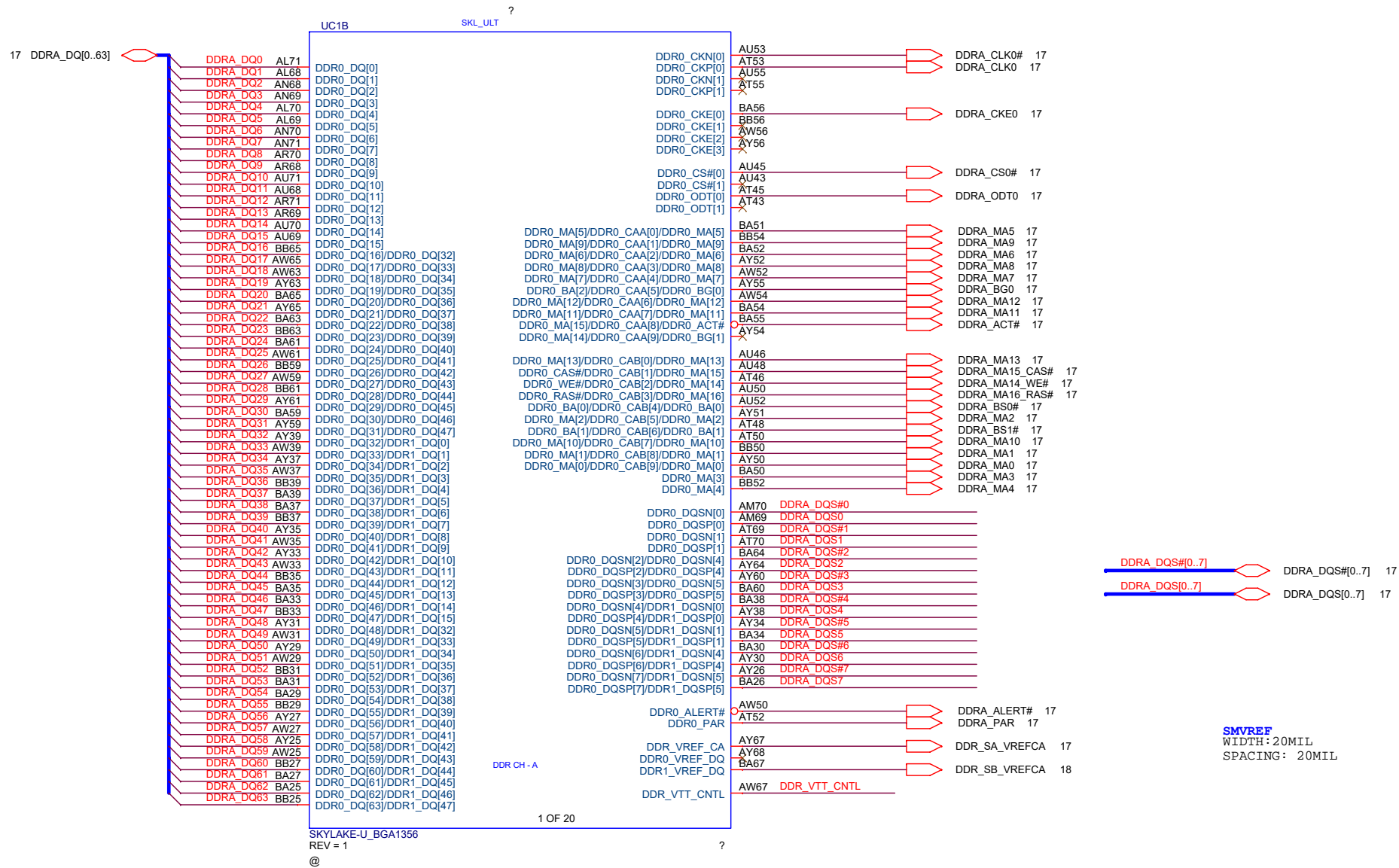
Sub-board(for 14")

- USB BOARD
- TP BOARD

Sub-board(for 15")

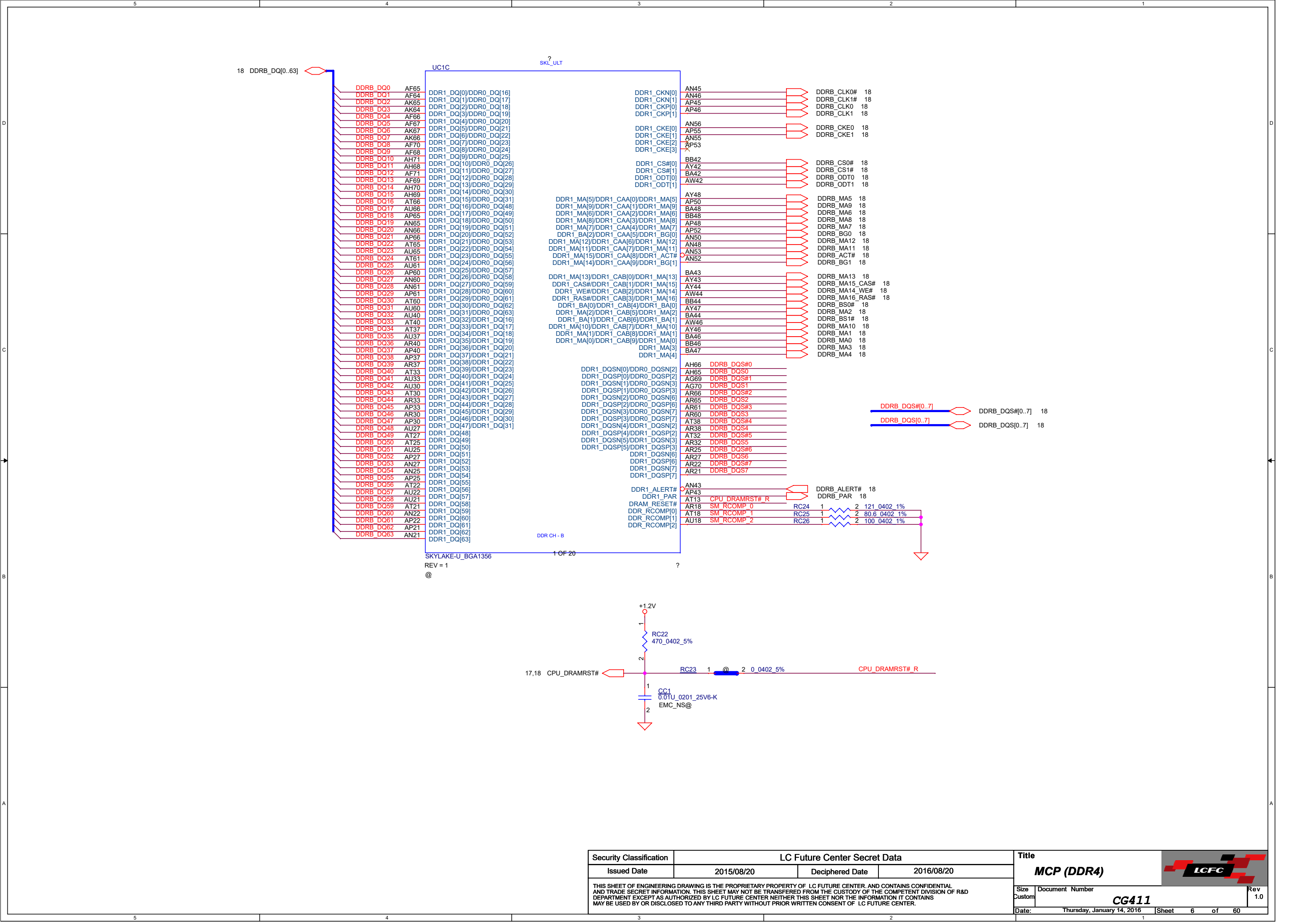
- USB BOARD
- TP BOARD
- ODD BOARD

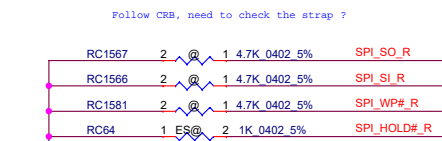
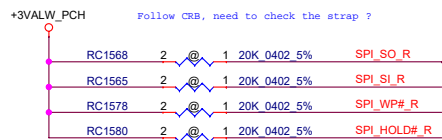
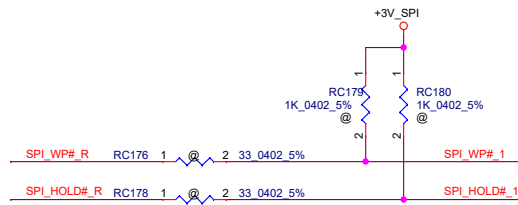
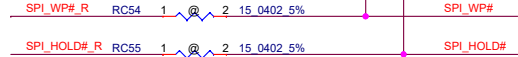
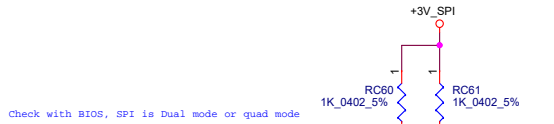
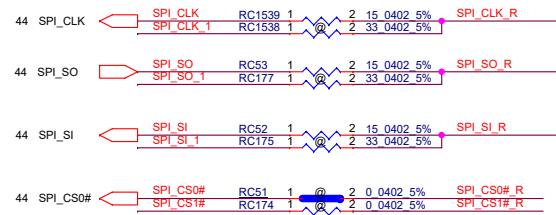




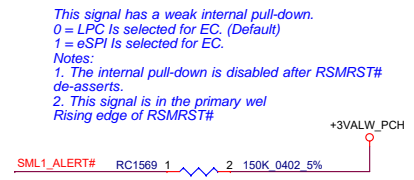
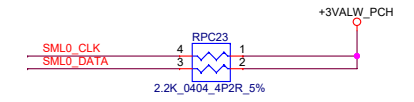
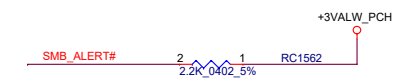
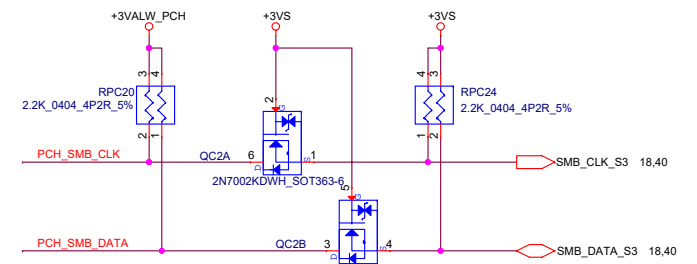
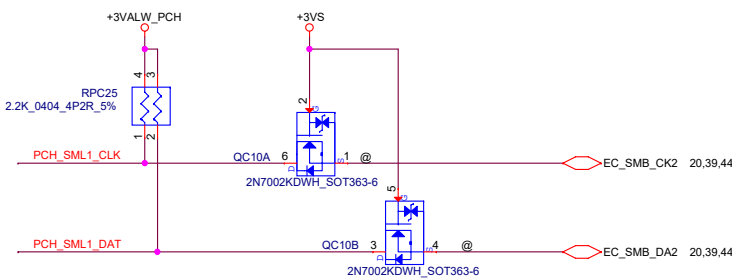
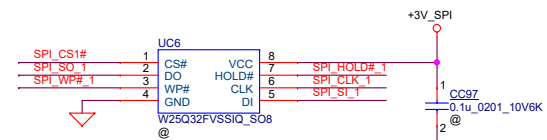
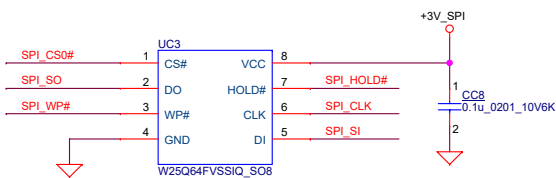
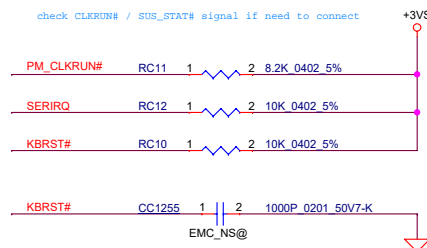
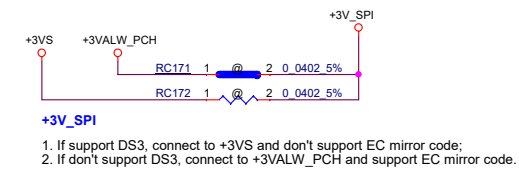
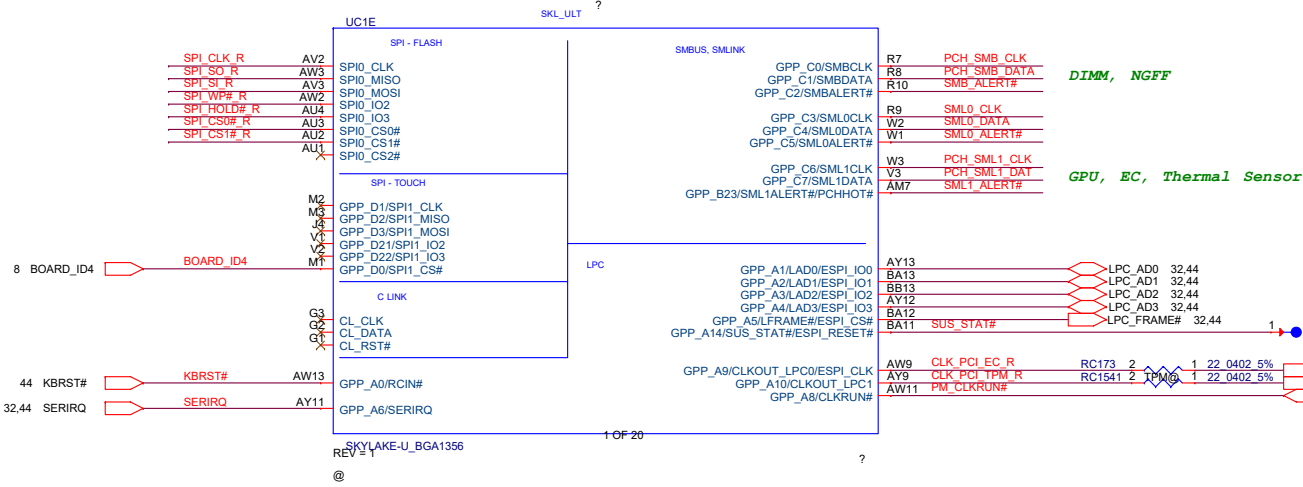
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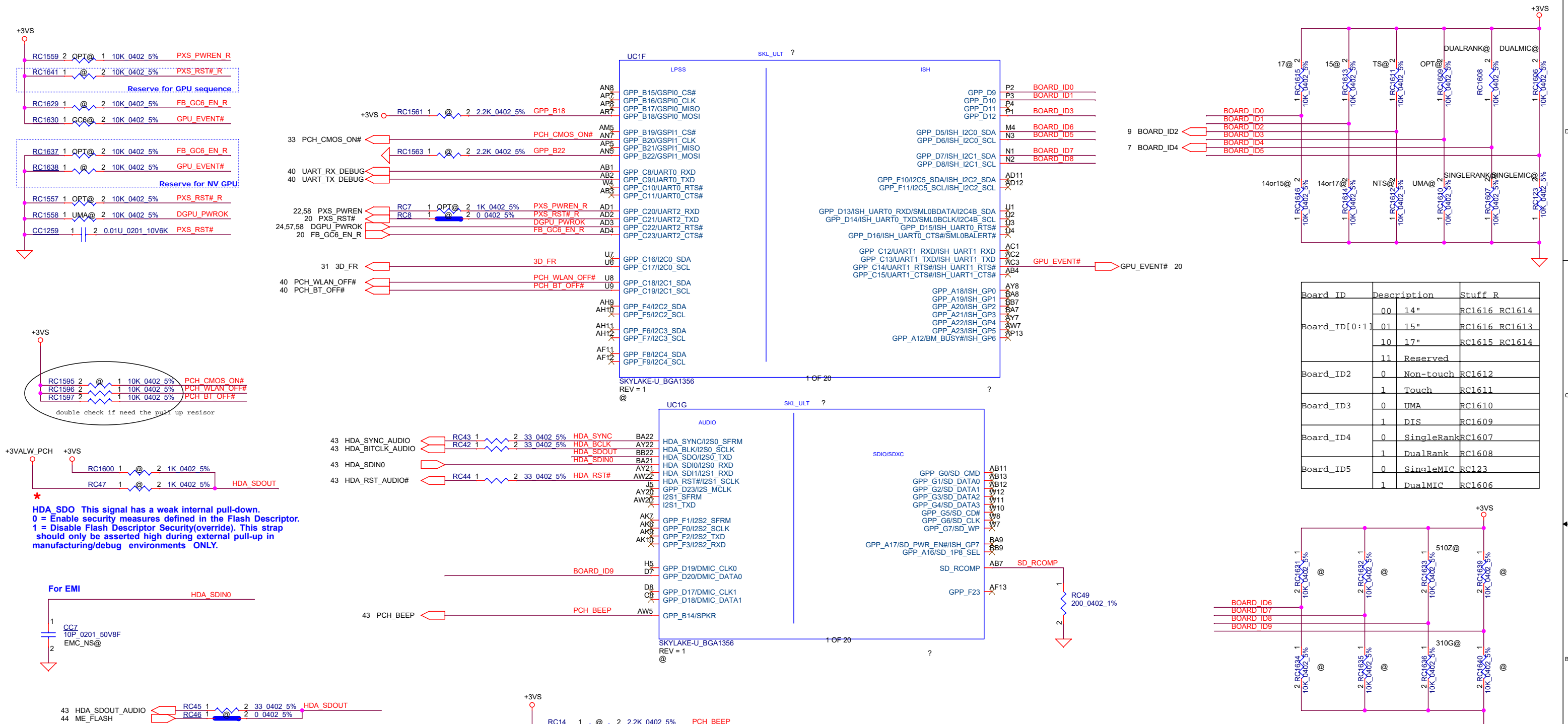


Based on WW36 SKL U&Y WOM, RC64 populated, and RC61 de-populated for SKL U ES sample. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.



To enable Direct Connect Interface (DCI), a 150K pull up resistor will need to be added to PCHHOT# pin. This pin must be low during the rising edge of RSMRST# (Refer to WWS2_MOW)

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Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable " Top Swap" mode. (Default) ★ 1 = Enable " Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0_MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable " No Reboot" mode. (Default) ★ 1 = Enable " No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1_MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) ★ 1 = LPC	0	Rising edge of PCH_PWROK

Security Classification

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Title

MCP (LPSS,ISH,AUDIO,SD)LCFC

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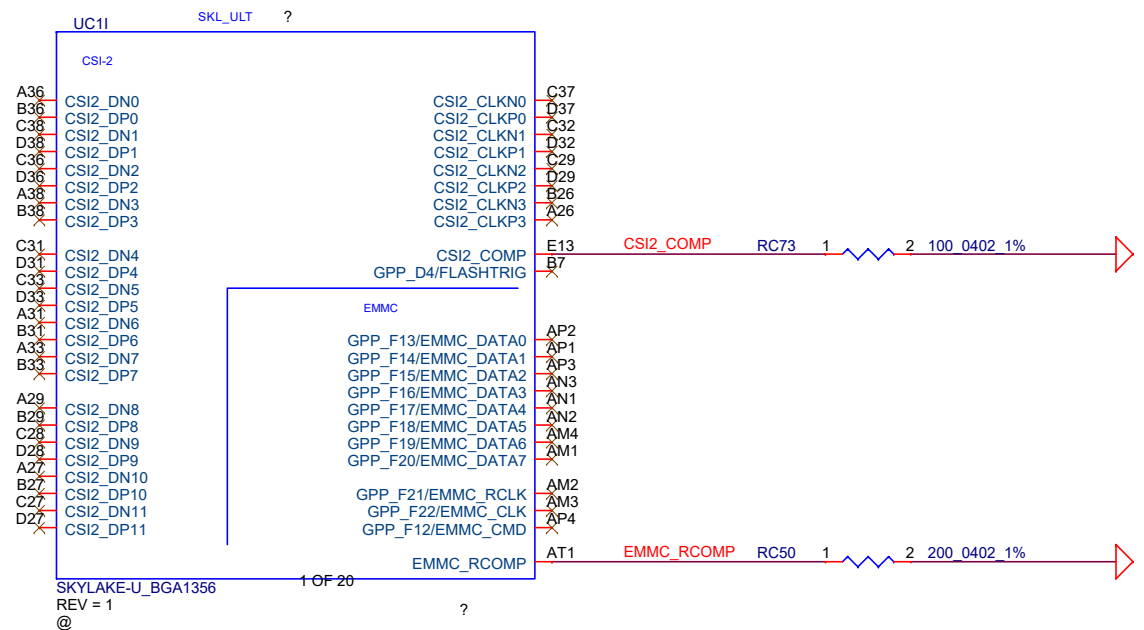
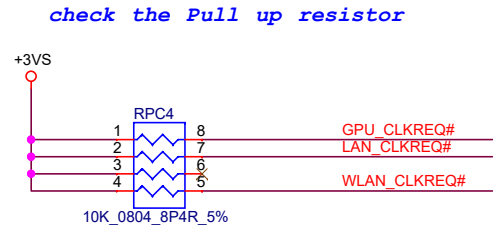
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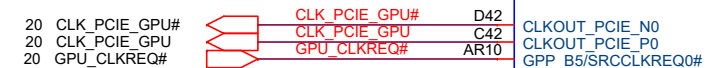
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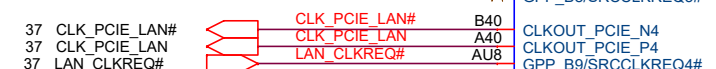
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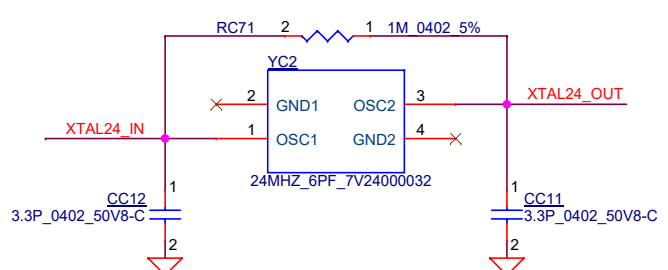
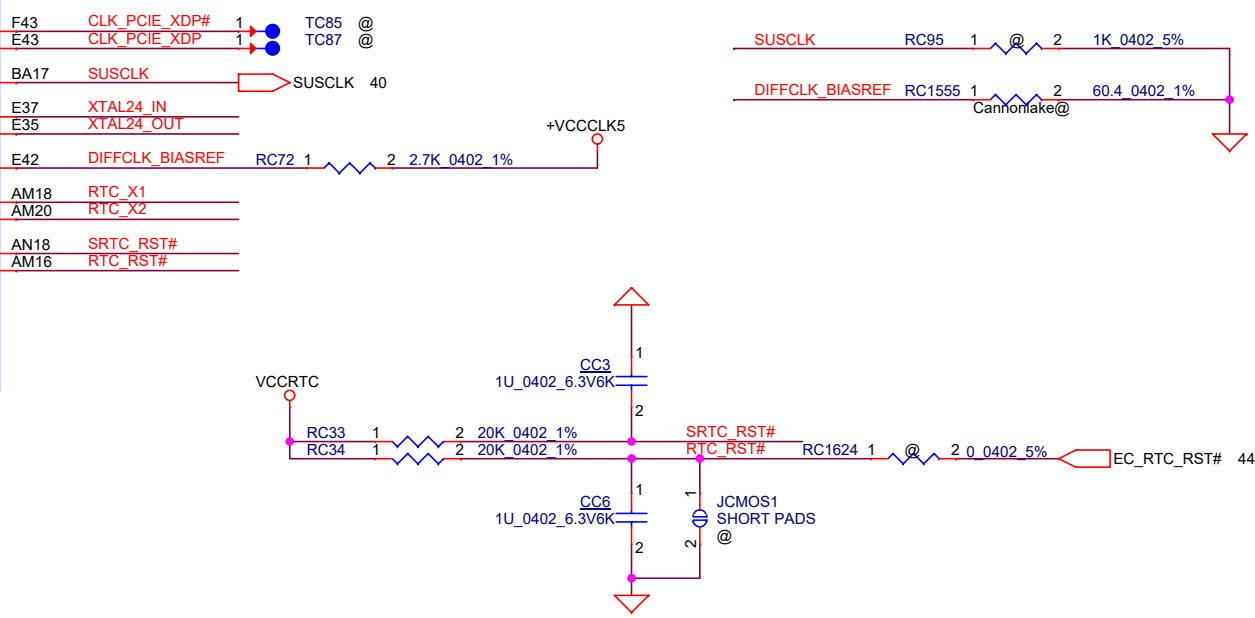
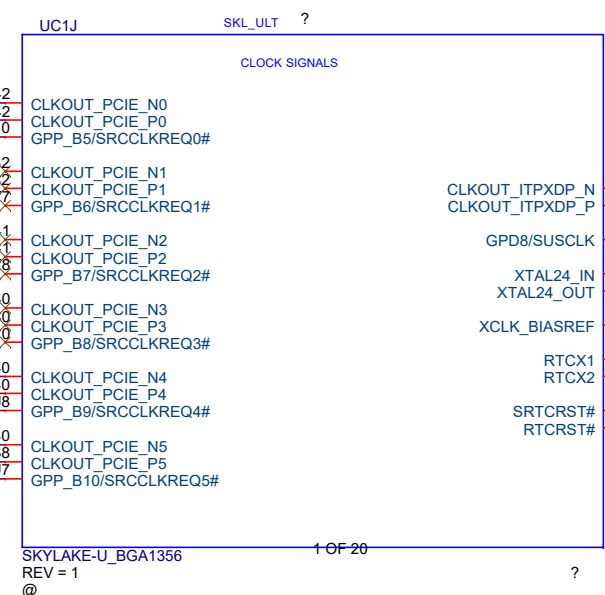
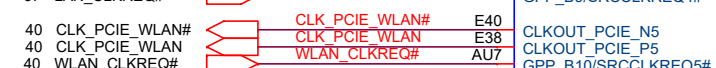
PCIE CLK0 DGPU



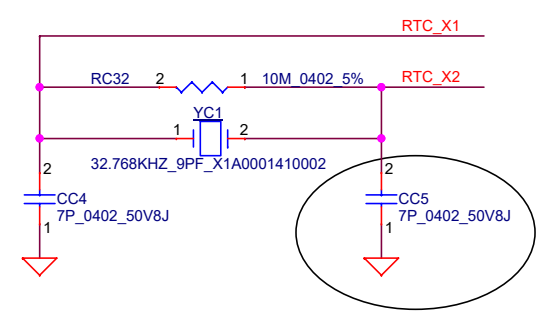
PCIE CLK4 LAN



PCIE CLK5 WLAN

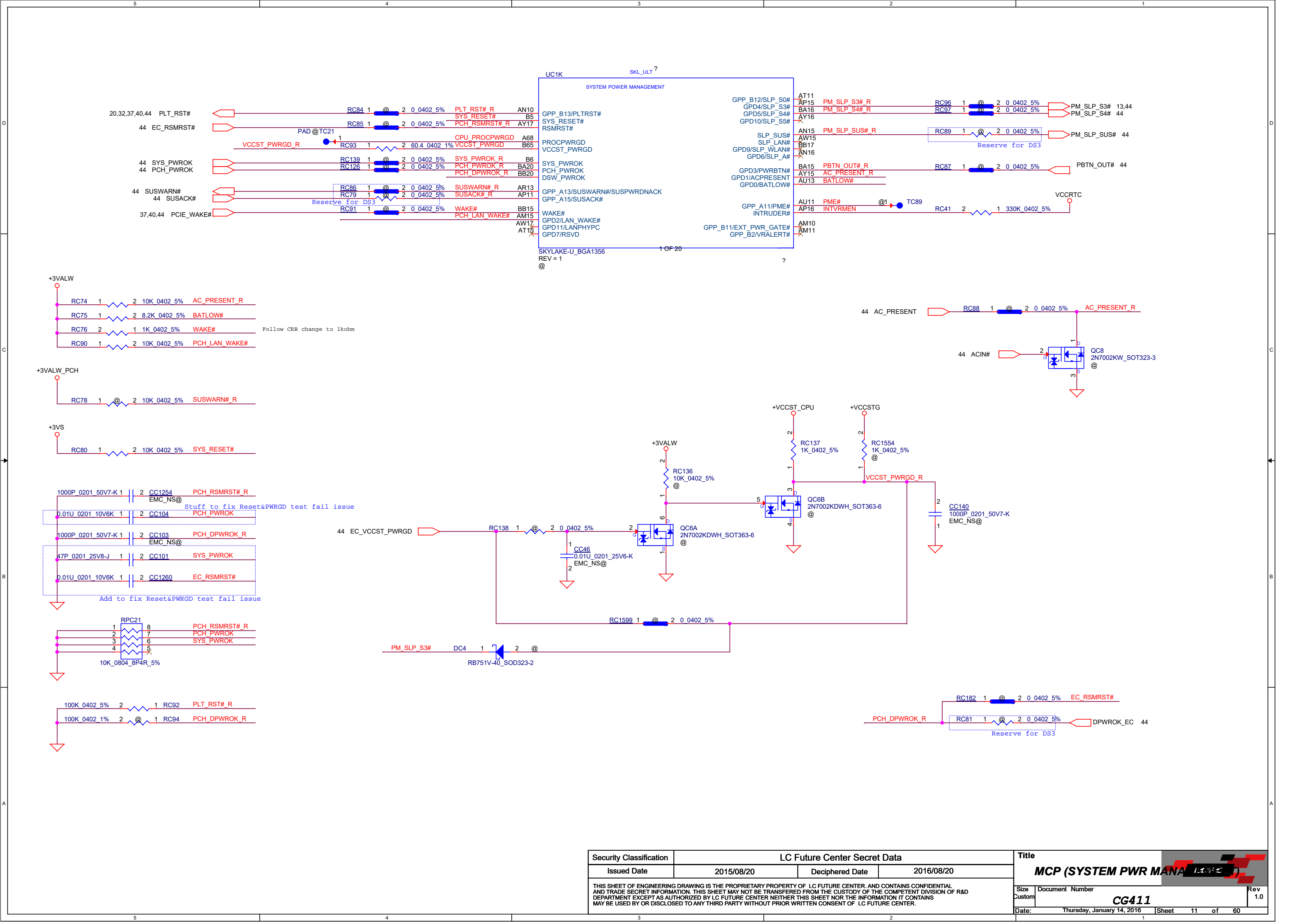


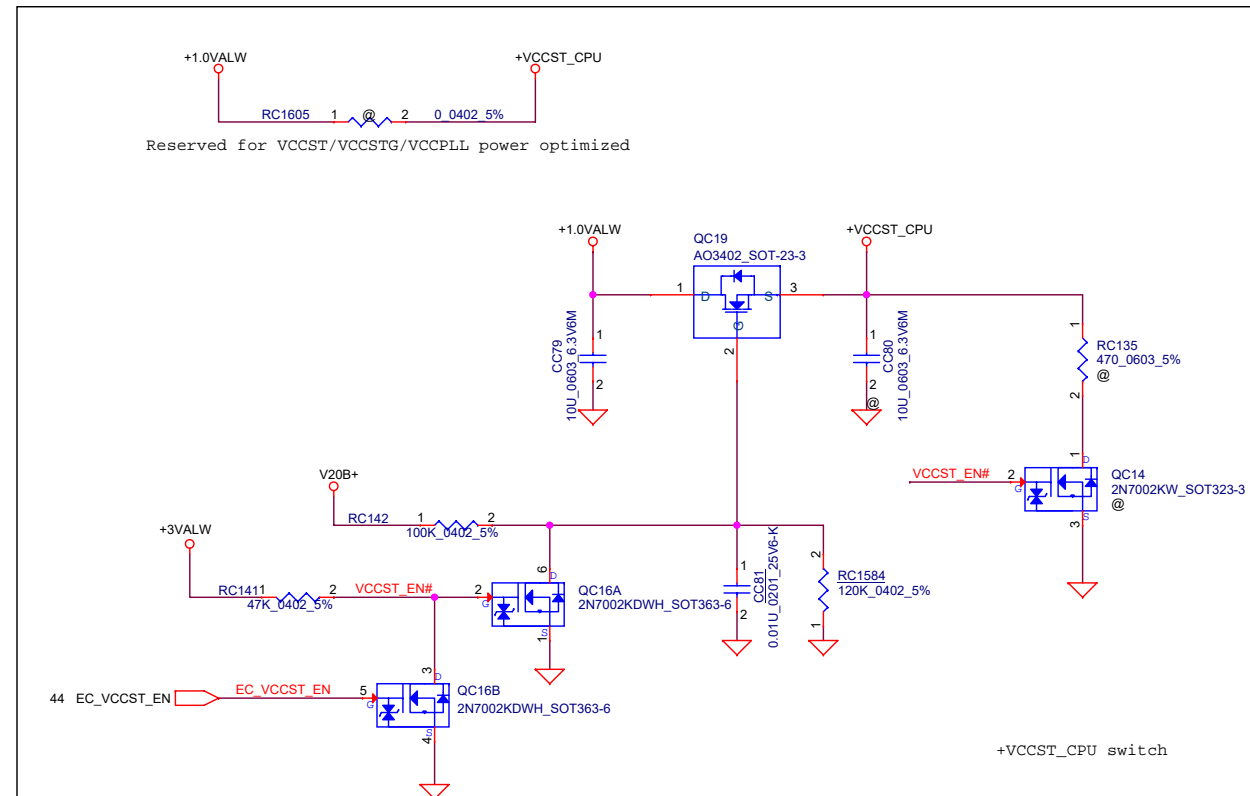
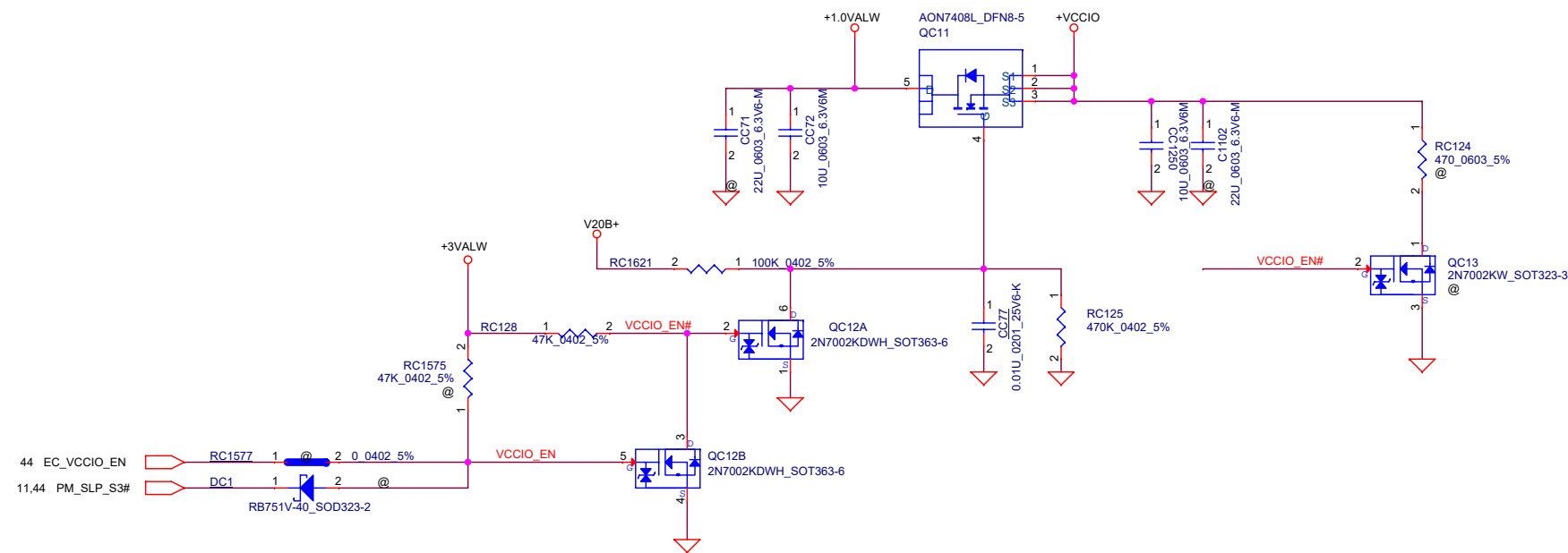
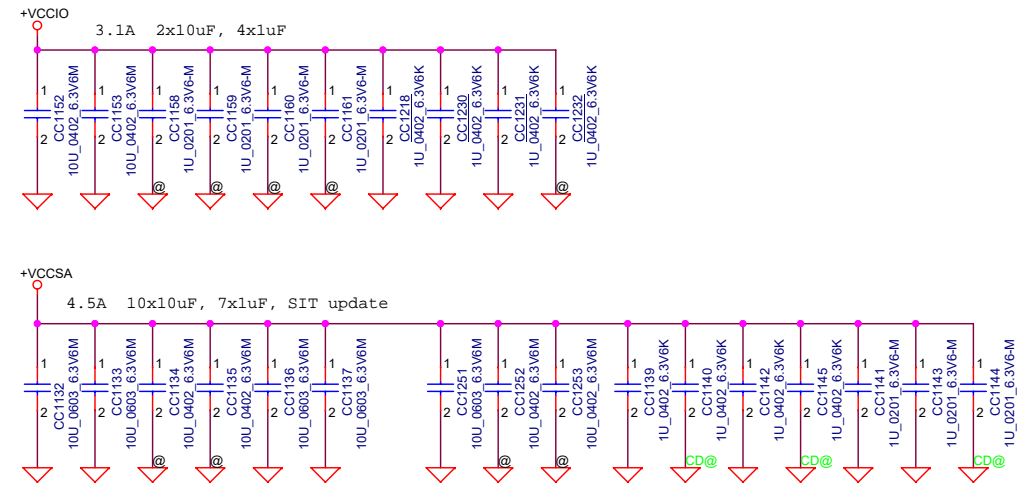
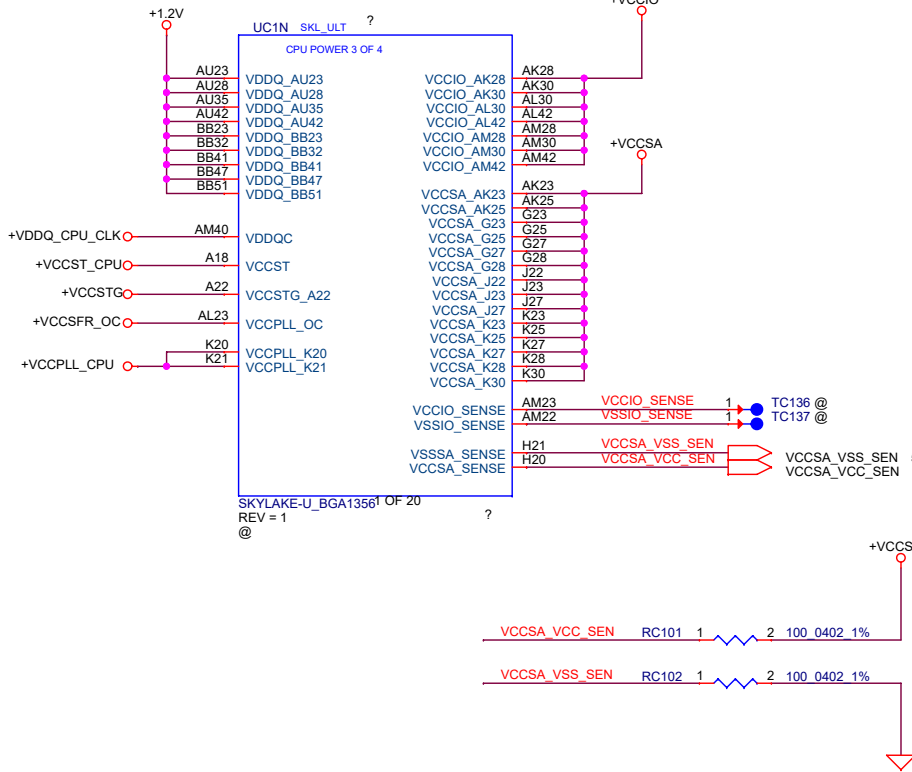
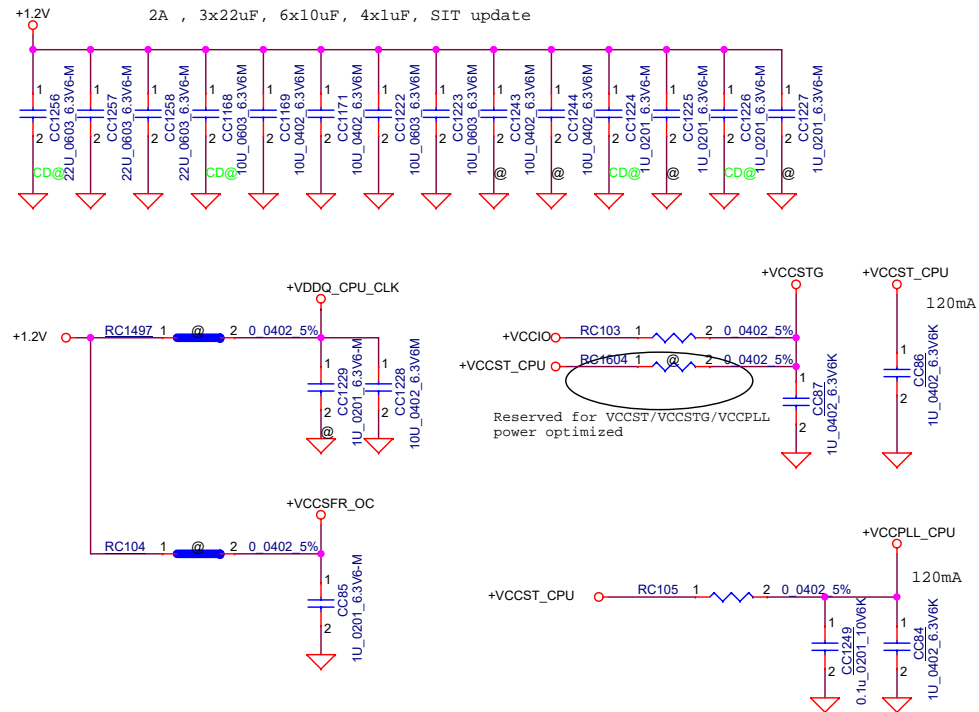
need to use 38.4MHz (30ohm) for Cannonlake-u




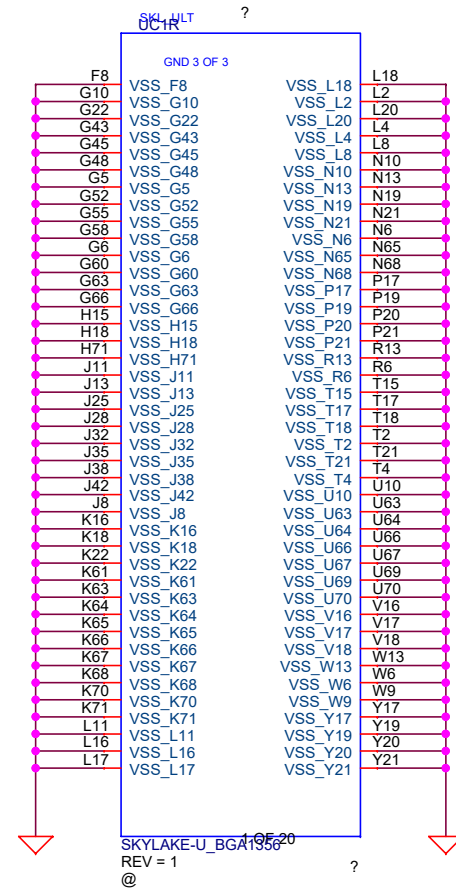
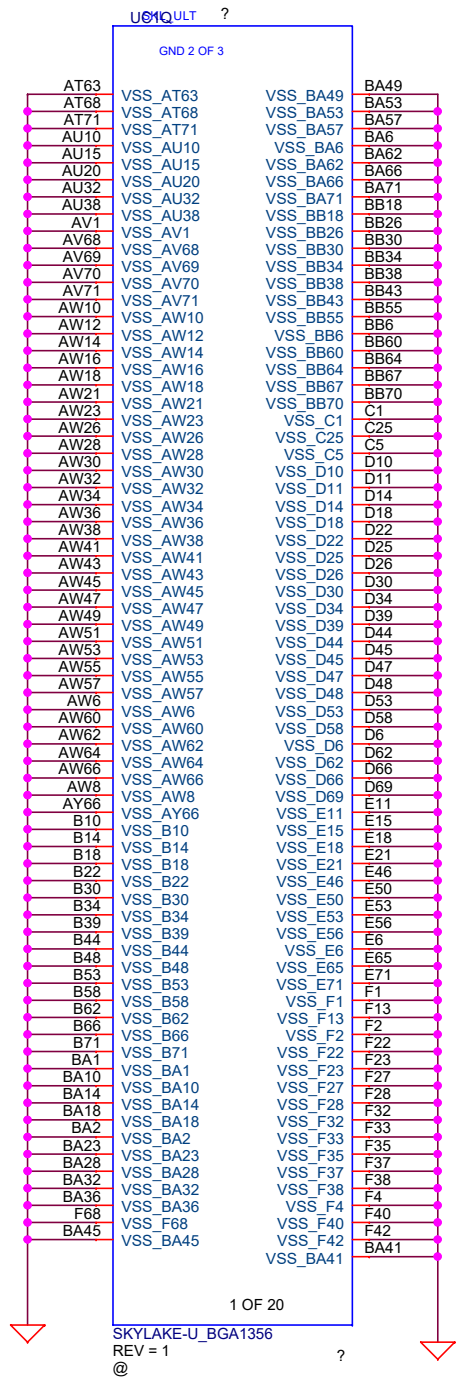
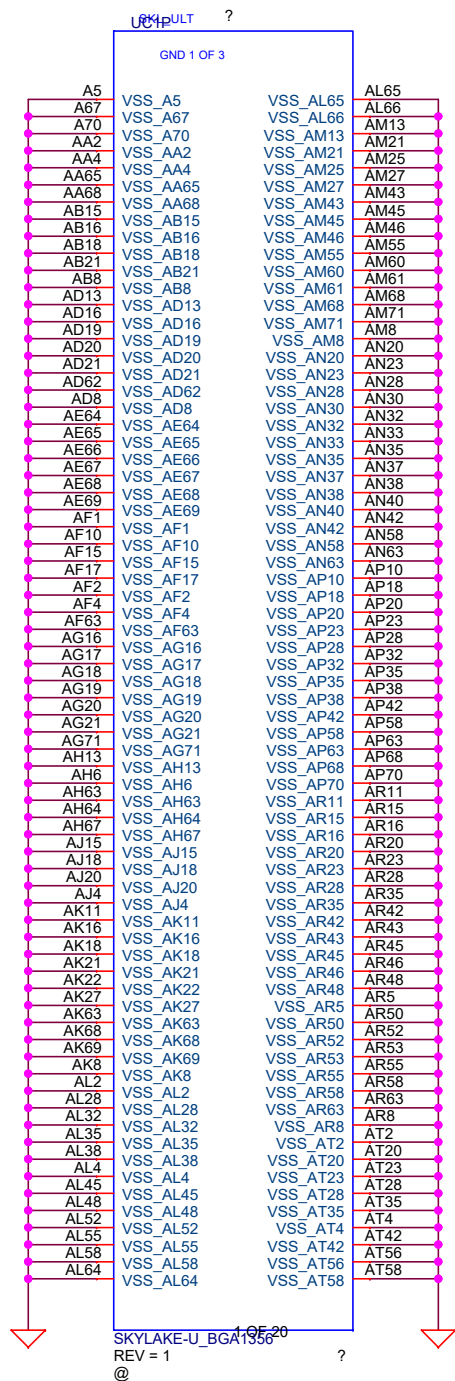
when single end external clock generator used, this pin should be grounded

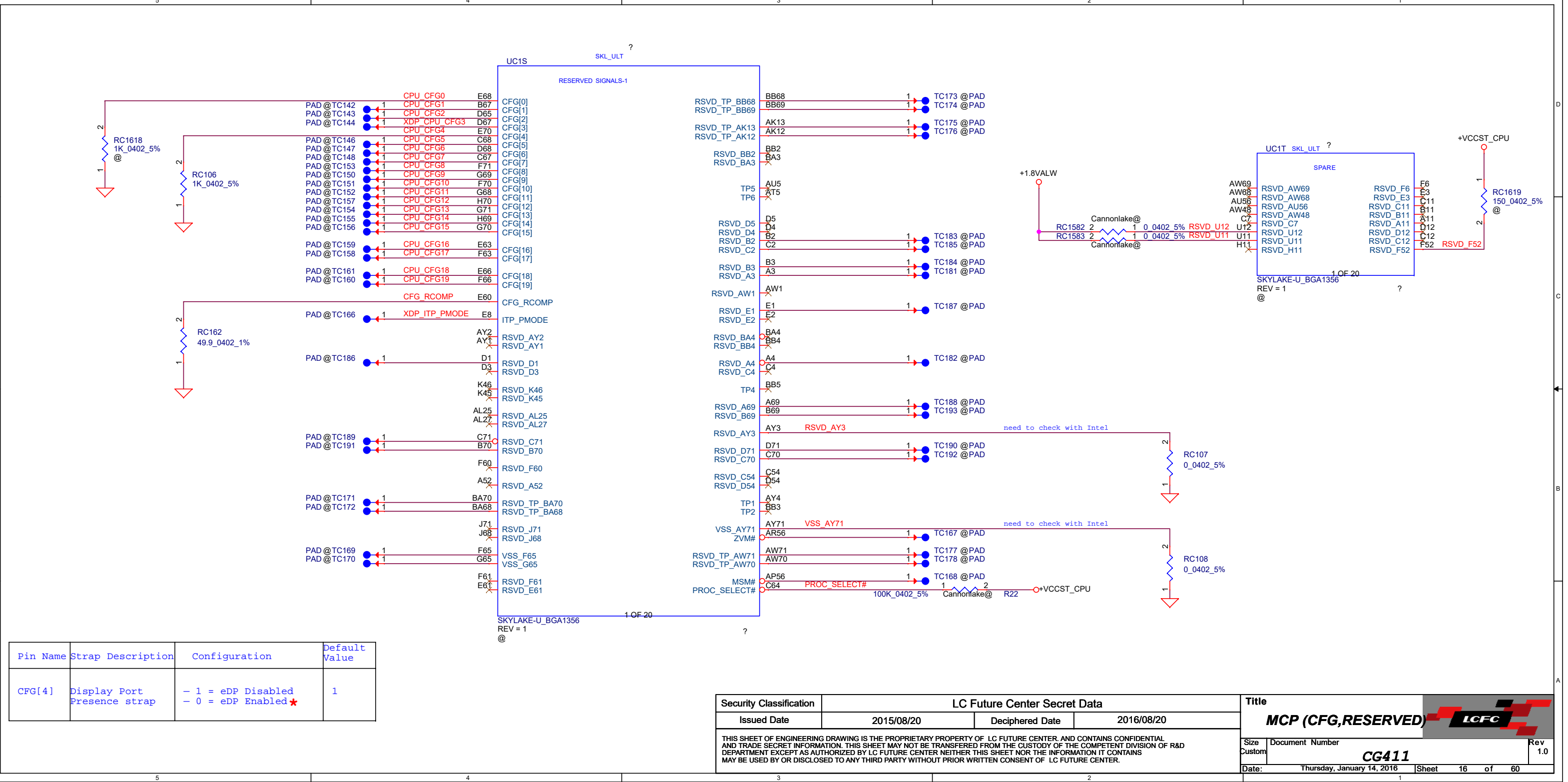
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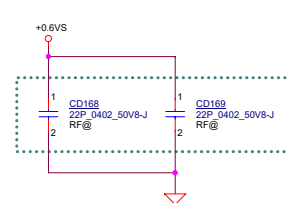
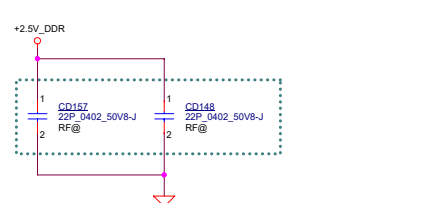
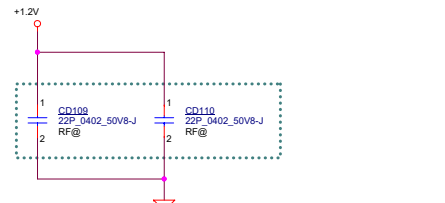
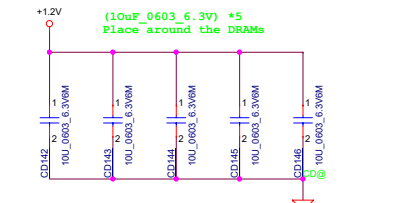
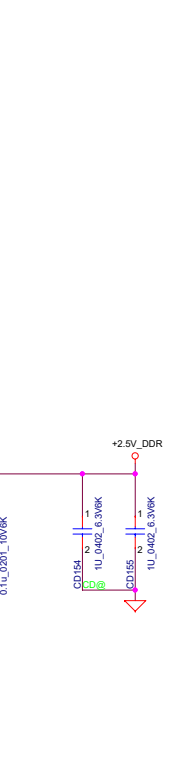
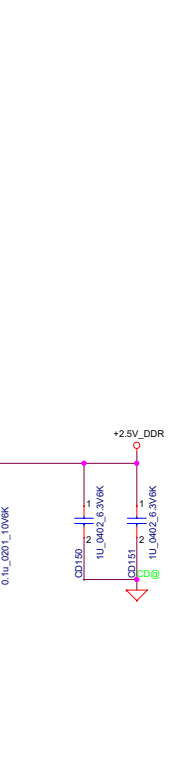
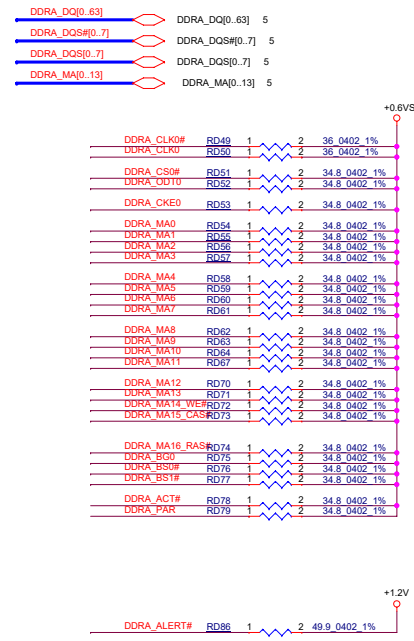
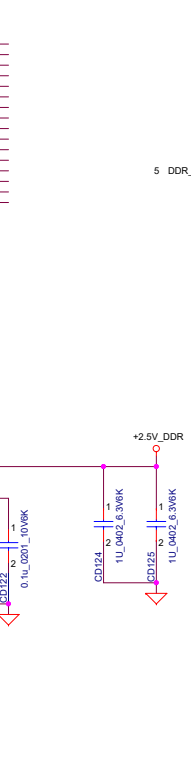
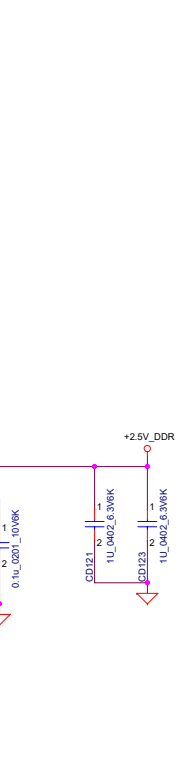



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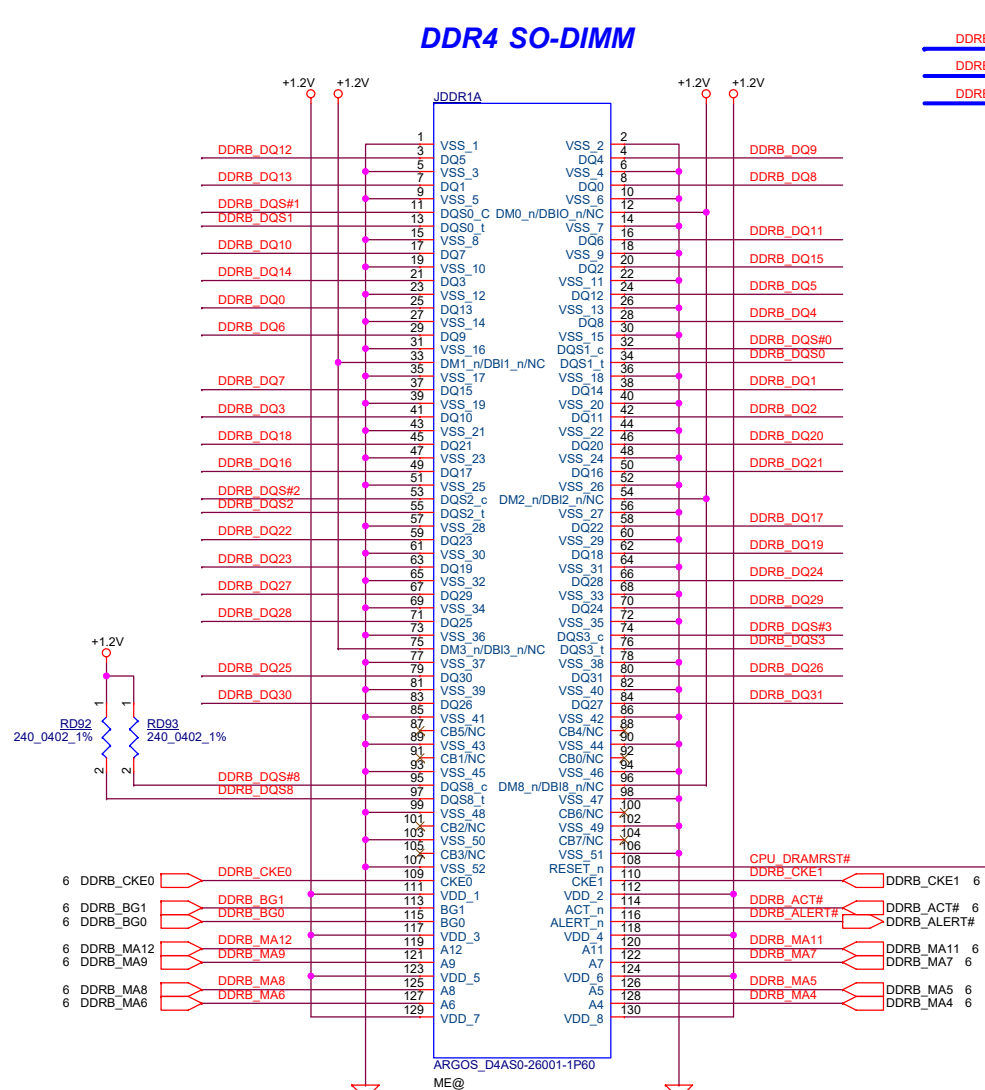


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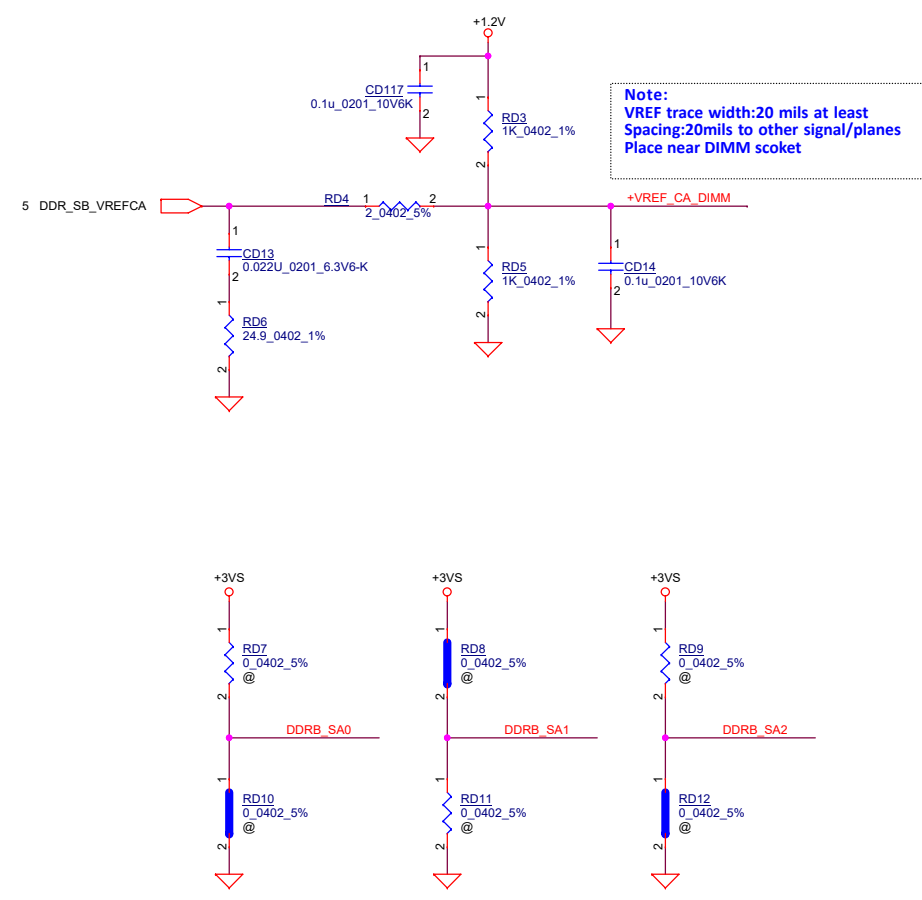
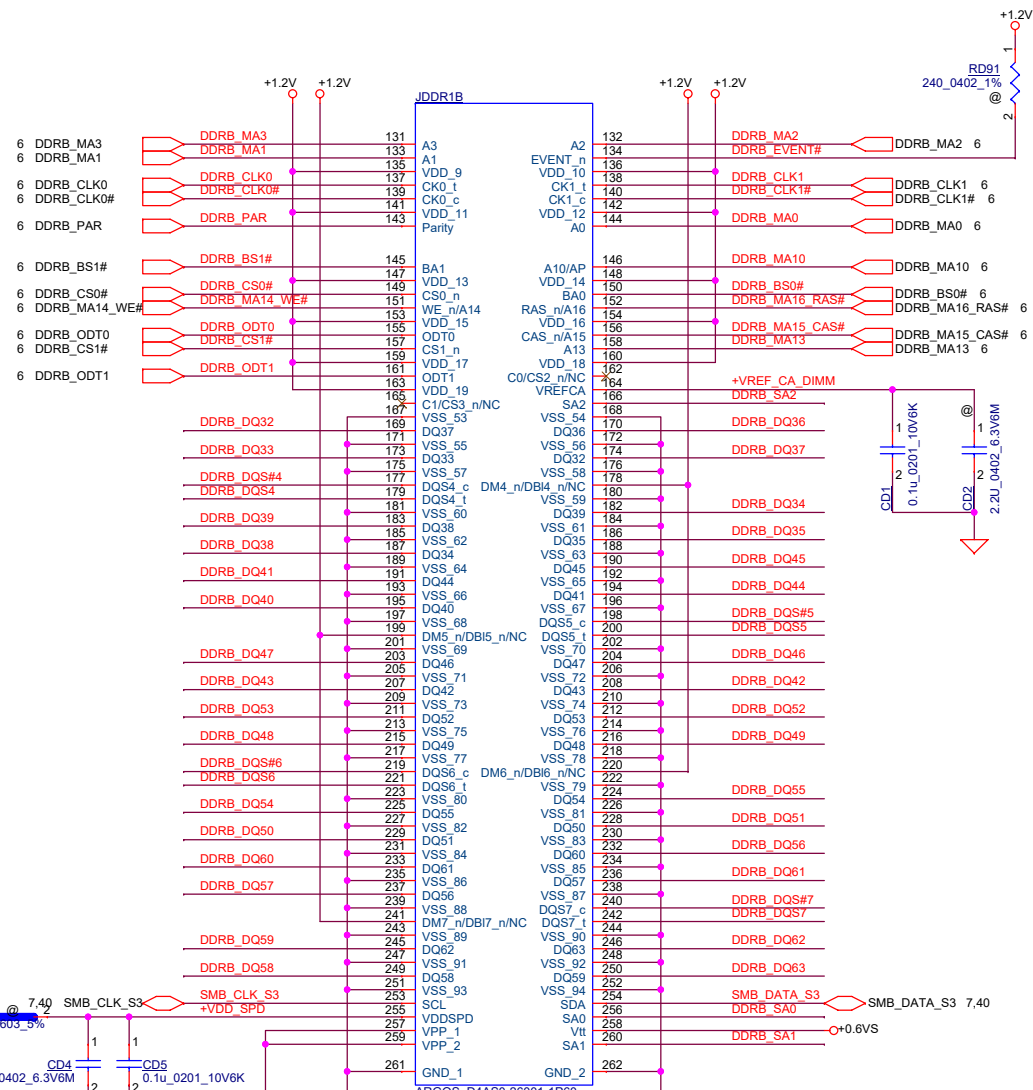


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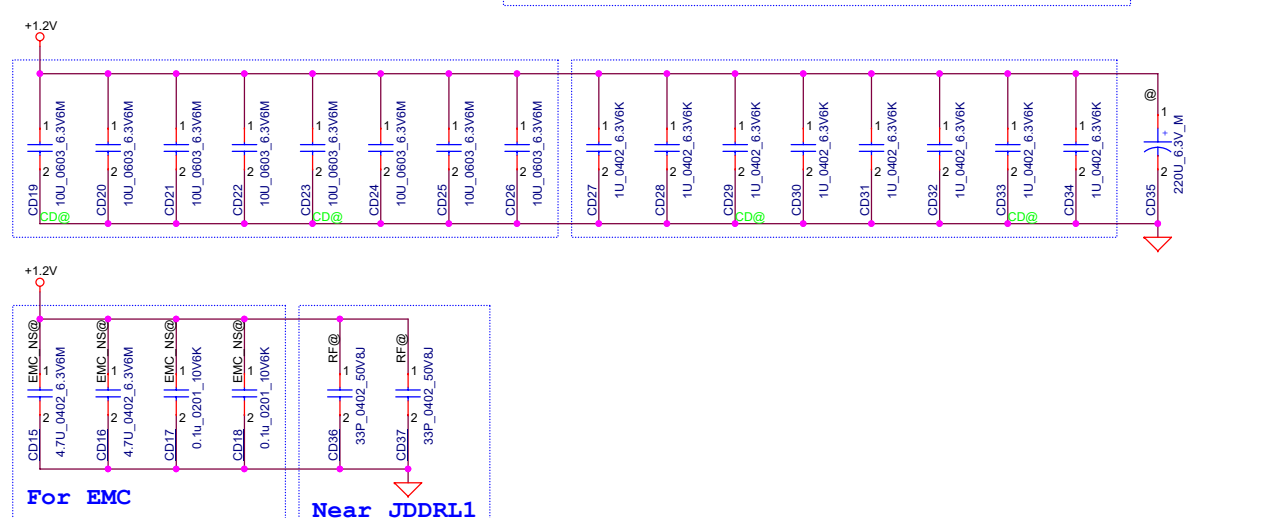
DDR4 SO-DIMM




DDRB_DQ[0..63] \rightarrow DDRB_DQ[0..63] 6
 DDRB_DQS[0..7] \rightarrow DDRB_DQS[0..7] 6
 DDRB_DQS[0..7] \rightarrow DDRB_DQS[0..7] 6



Layout Note:
Place near DIMM



SPD Address = 2H

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N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

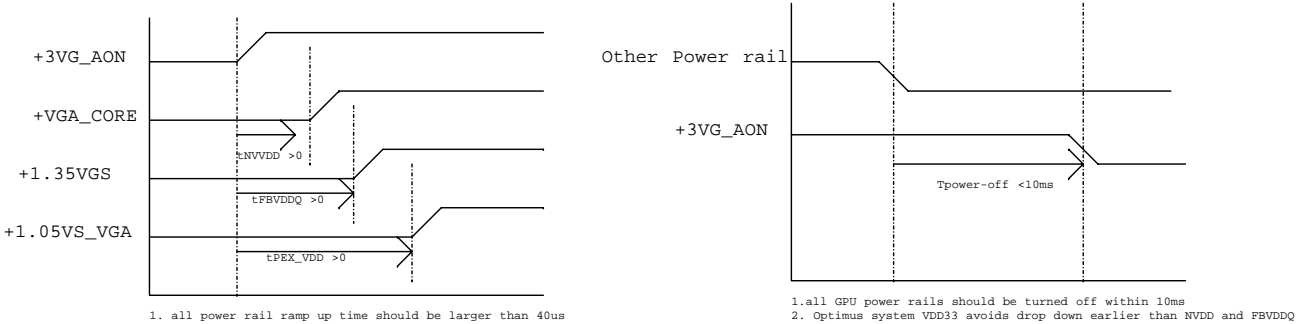
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)			I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)		(mA)	(W)	(mA)	(W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD		TBD	TBD	TBD	TBD

N15x Multi-level Straps

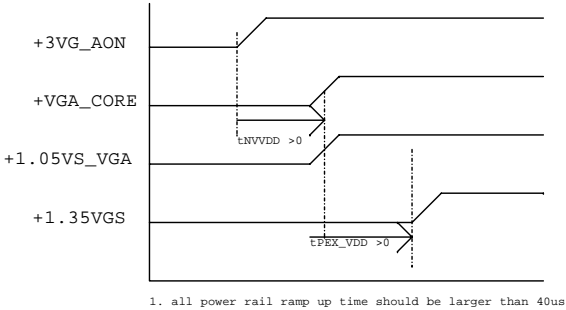
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCI_E_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15V-GM Power Sequence

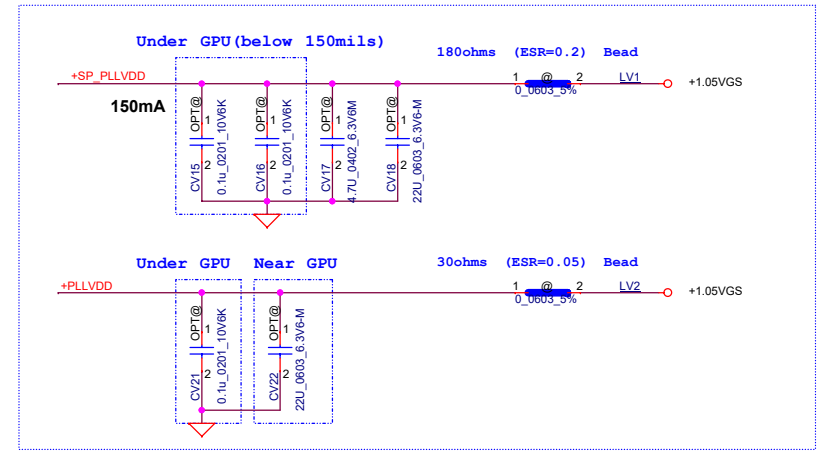
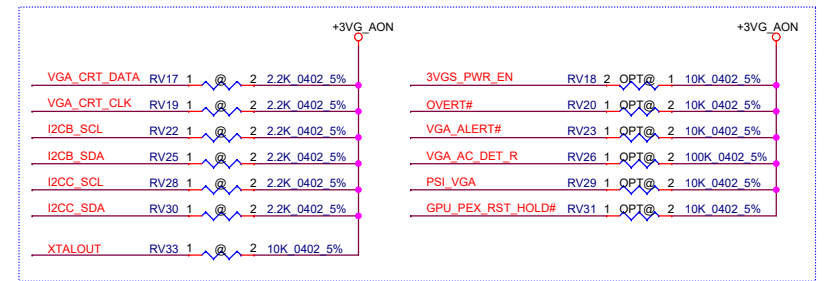
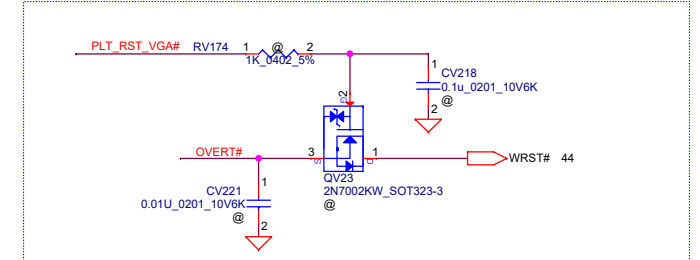
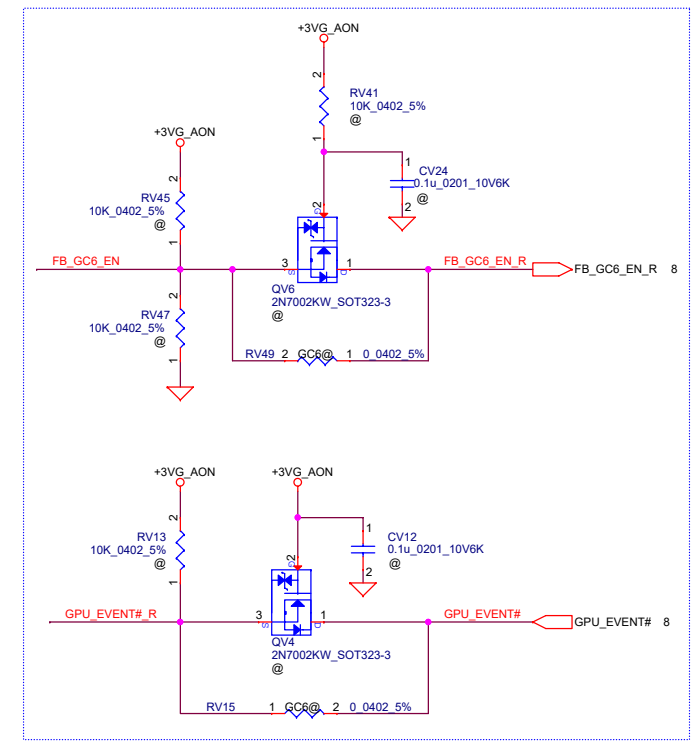
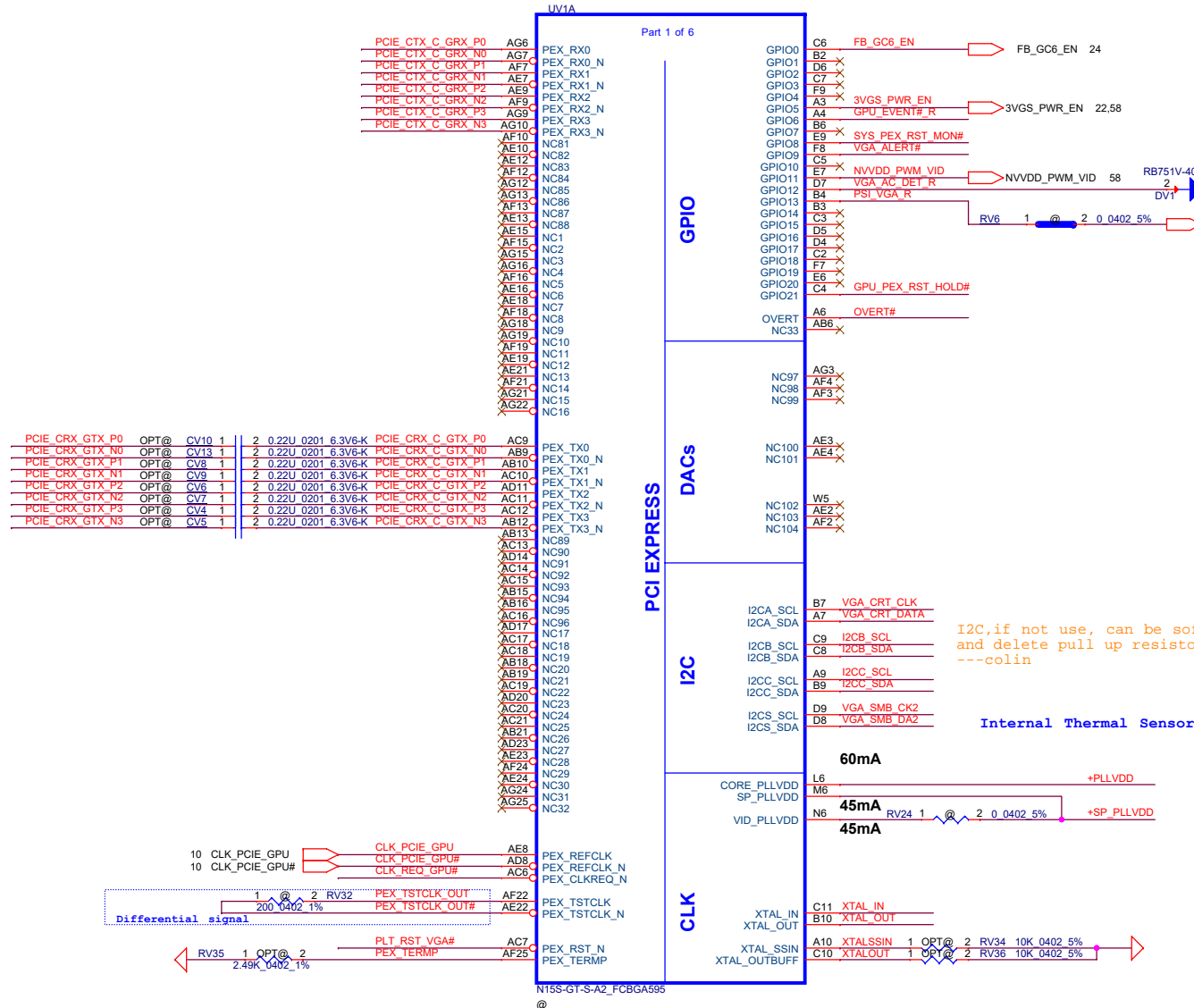
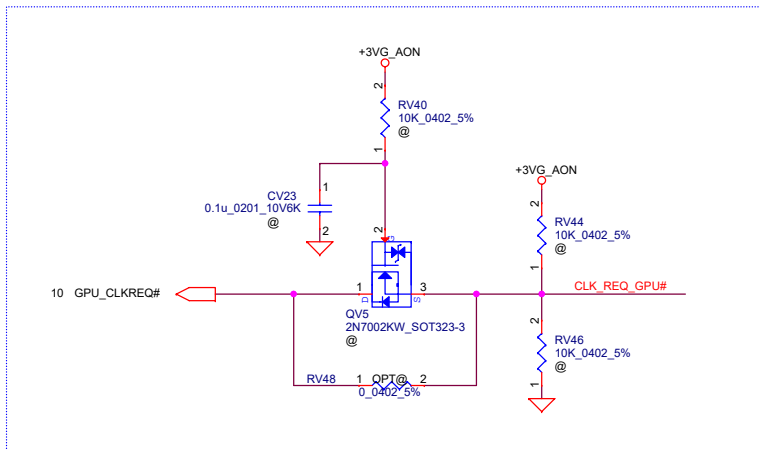




N15S-GT Power Sequence

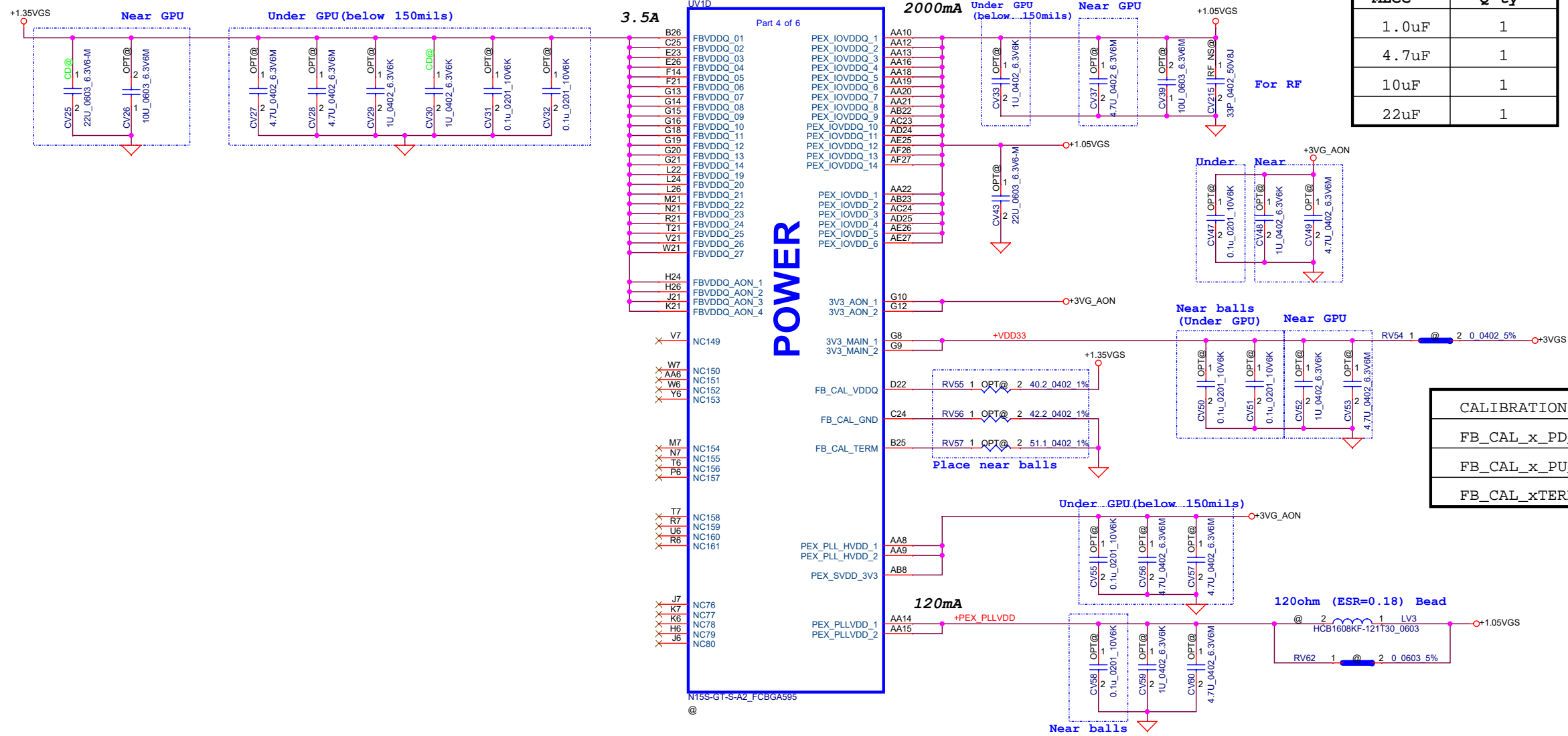


N15x Binary Straps

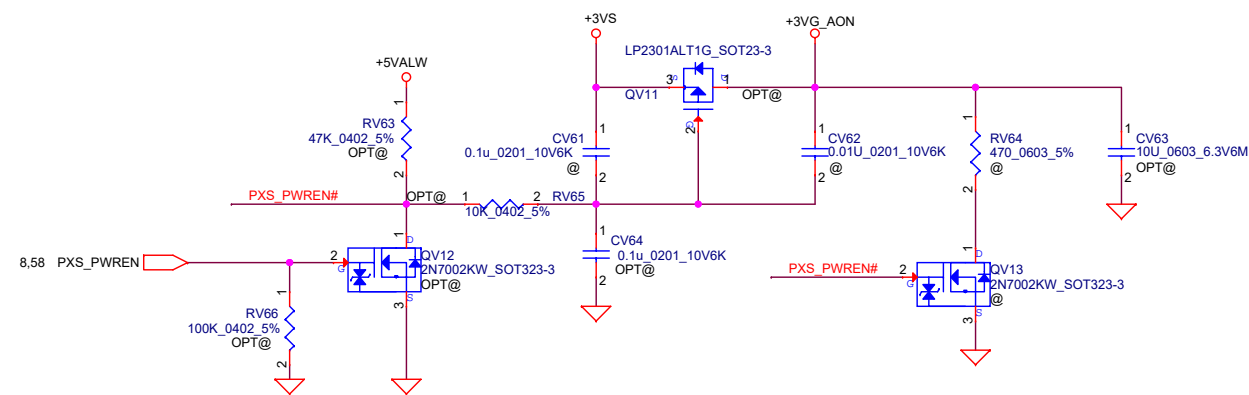
Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCI_E_MAX_SPEED



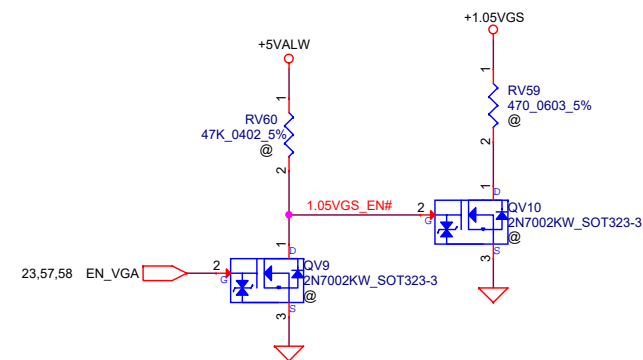
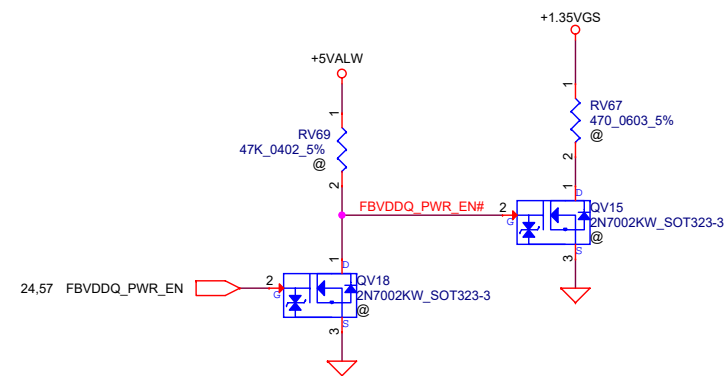
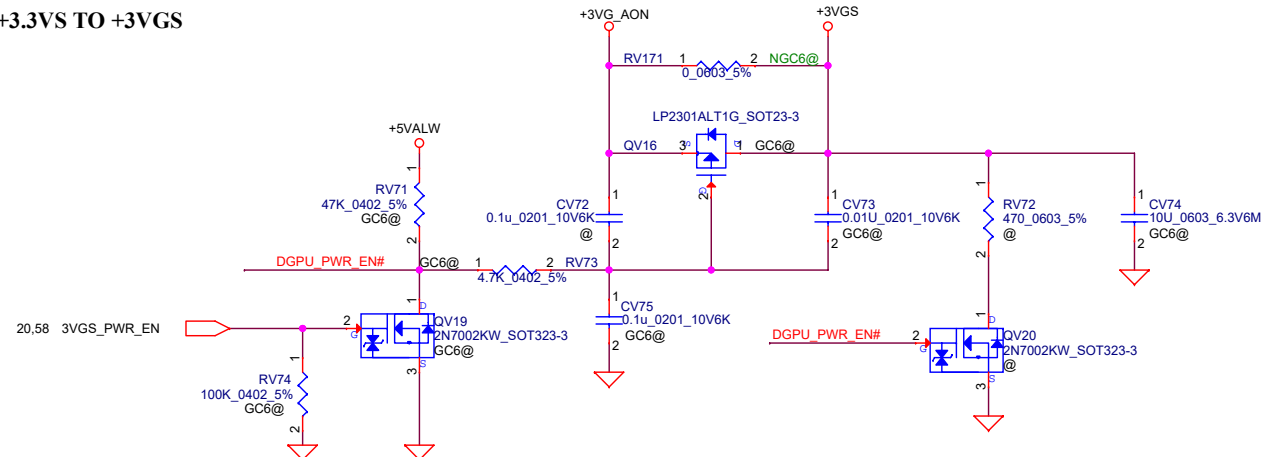
Security Classification		LC Future Center Secret Data		Title			
Issued Date		Deciphered Date		N16X_PCIE/ DAC/ GPIO			
2015/08/20		2016/08/20		Size Document Number Custom CG411		Rev 1.0	
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		2		1			

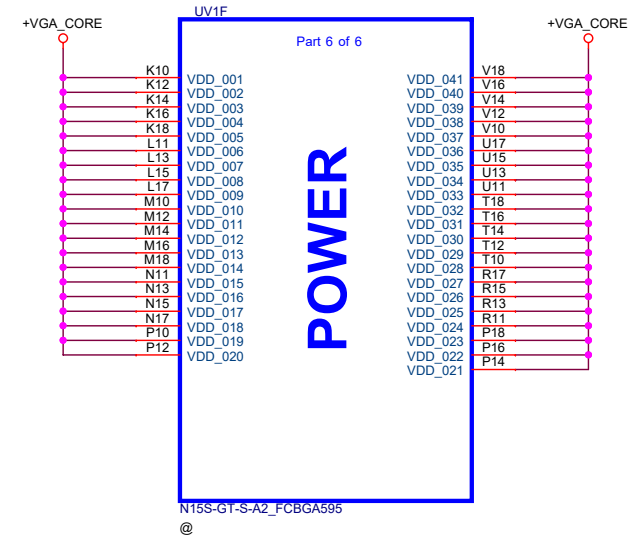
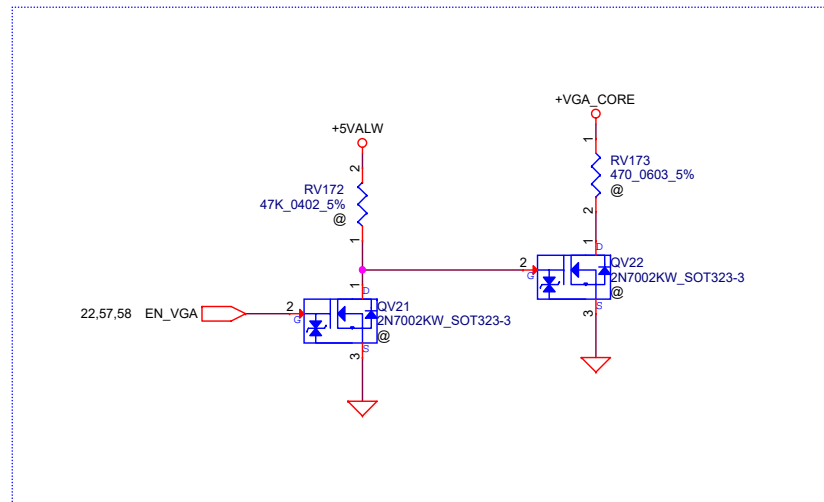
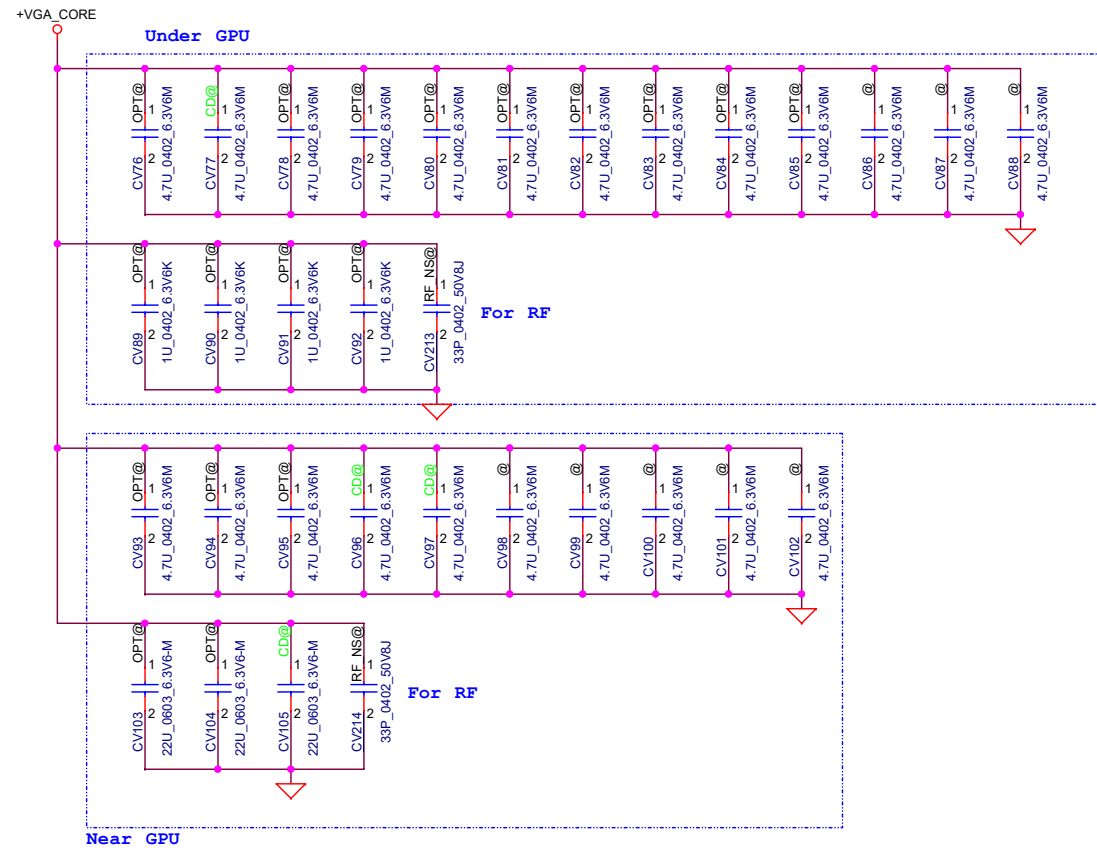
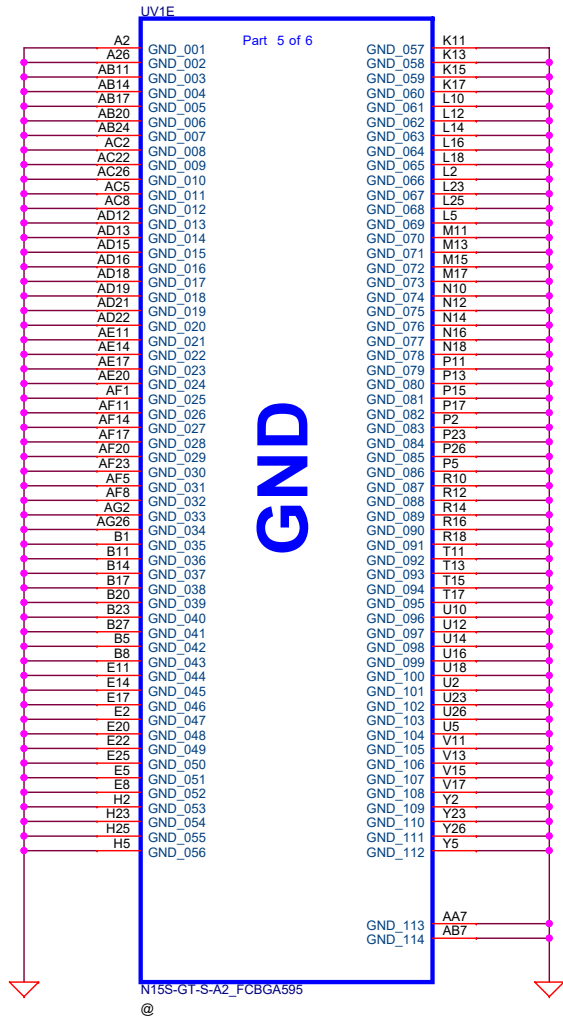


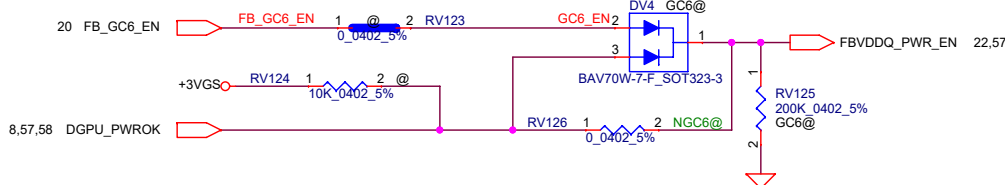
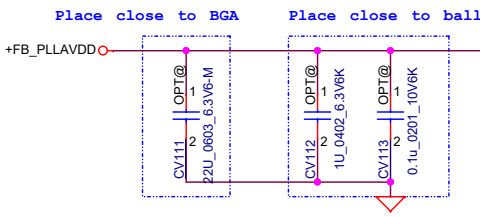
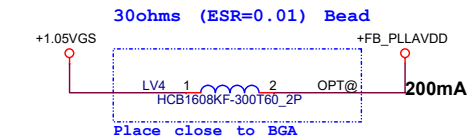
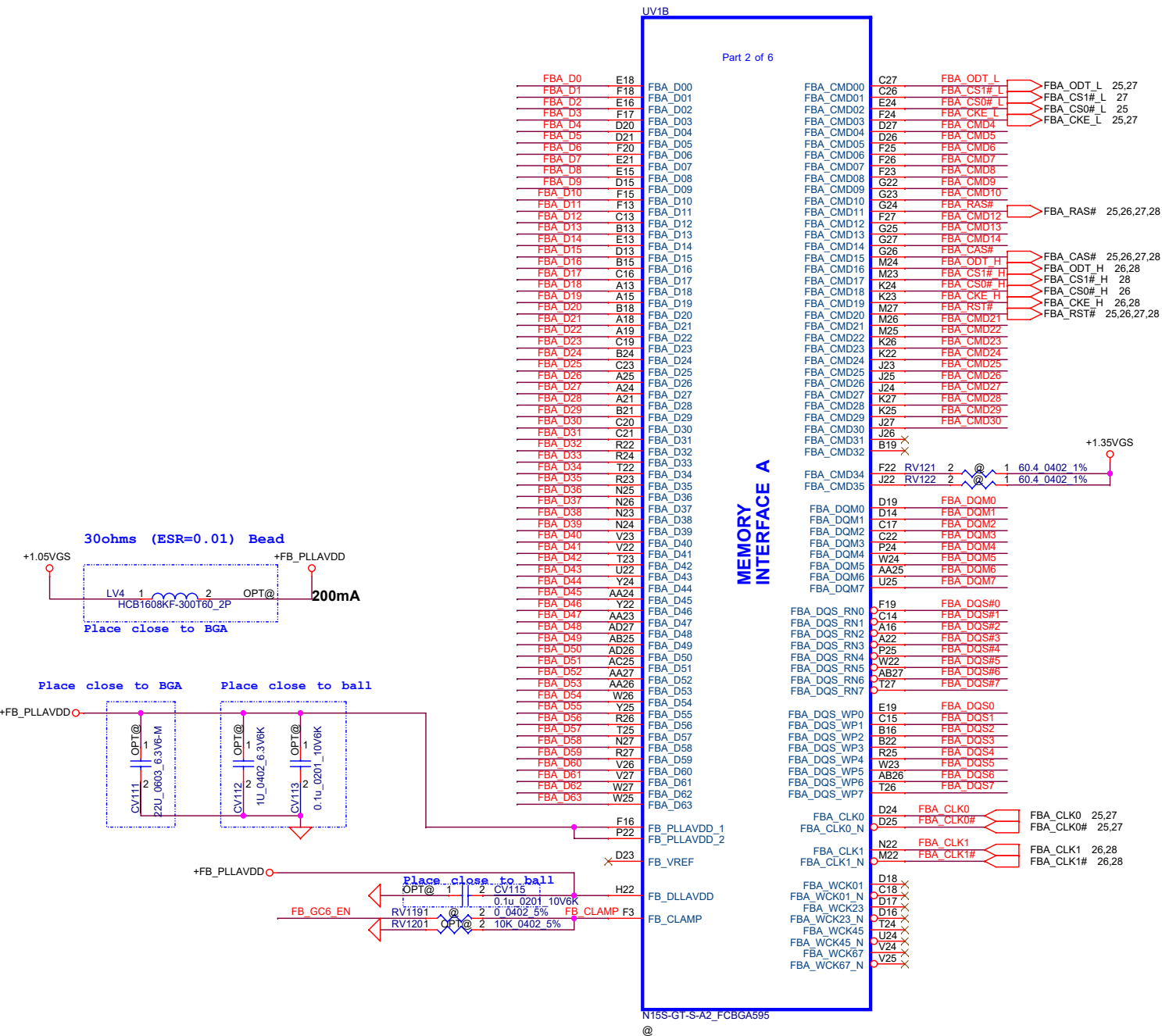
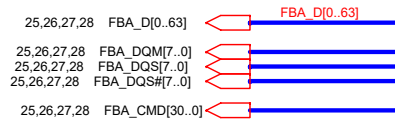
+3.3VS TO +3VG_AON



+3.3VS TO +3VGS

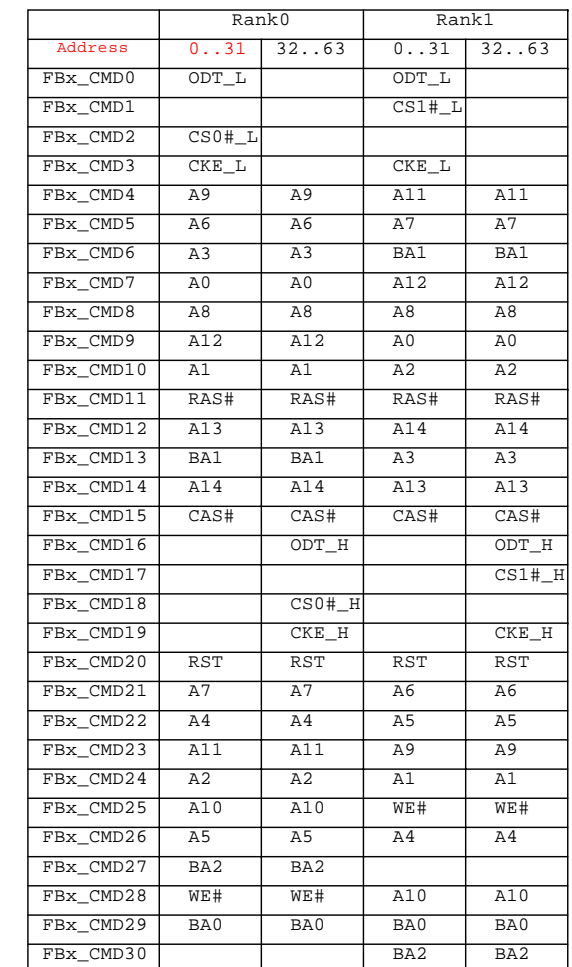
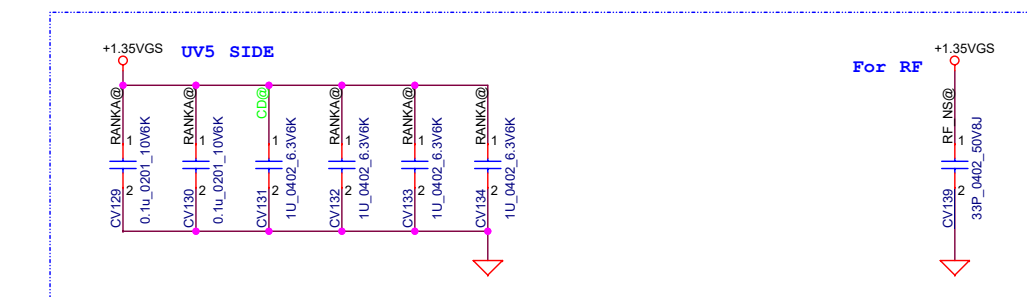
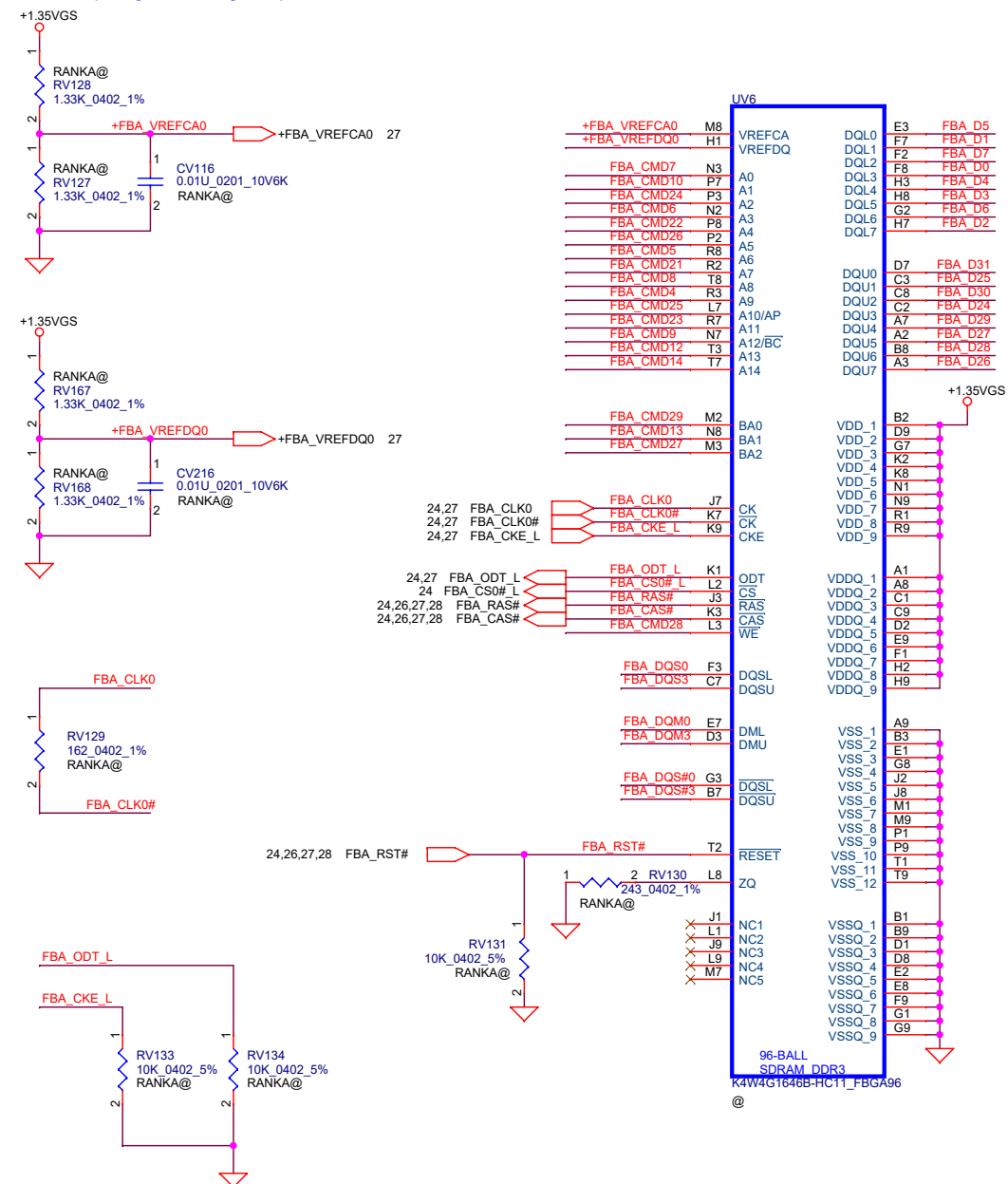




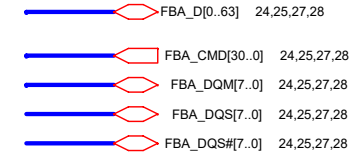
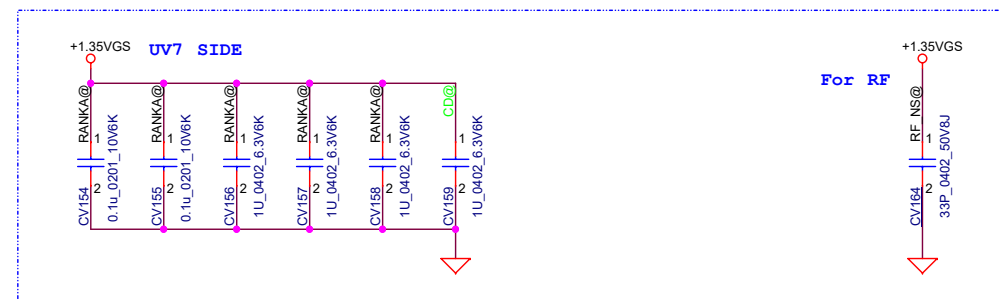
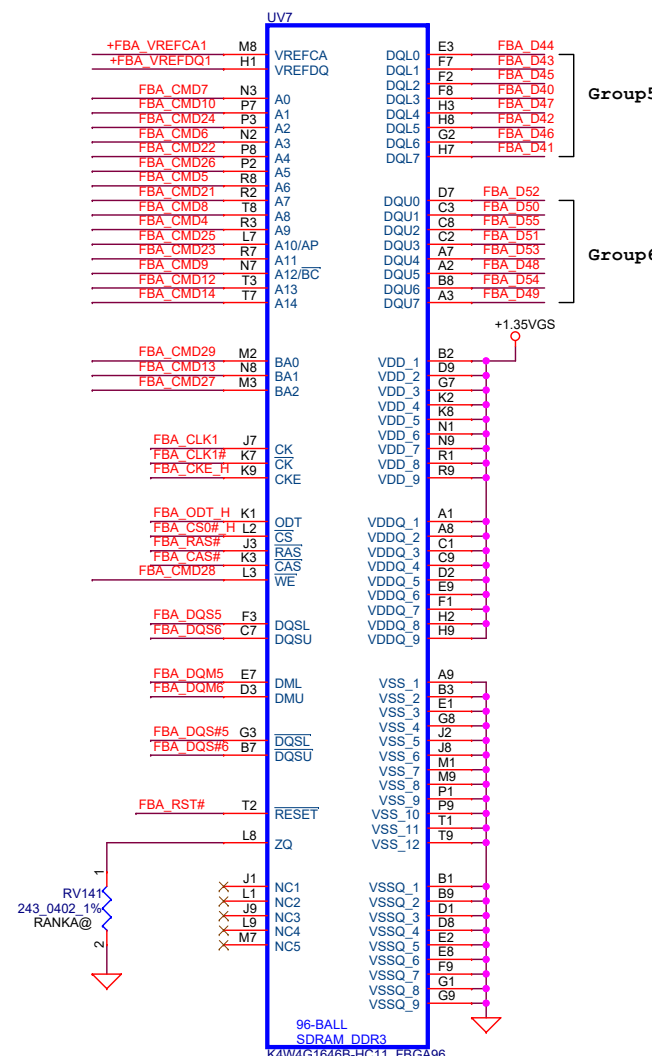
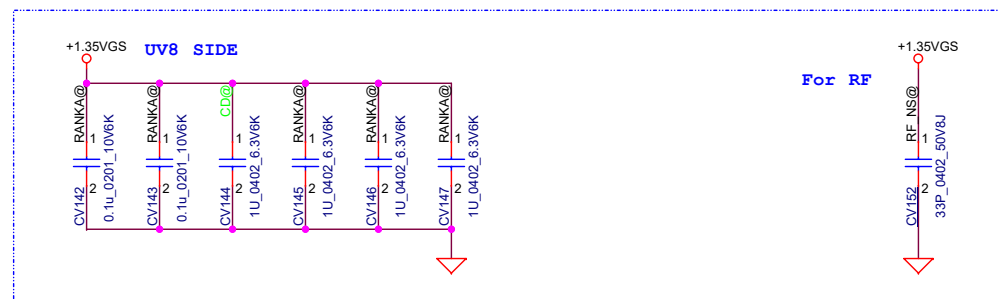
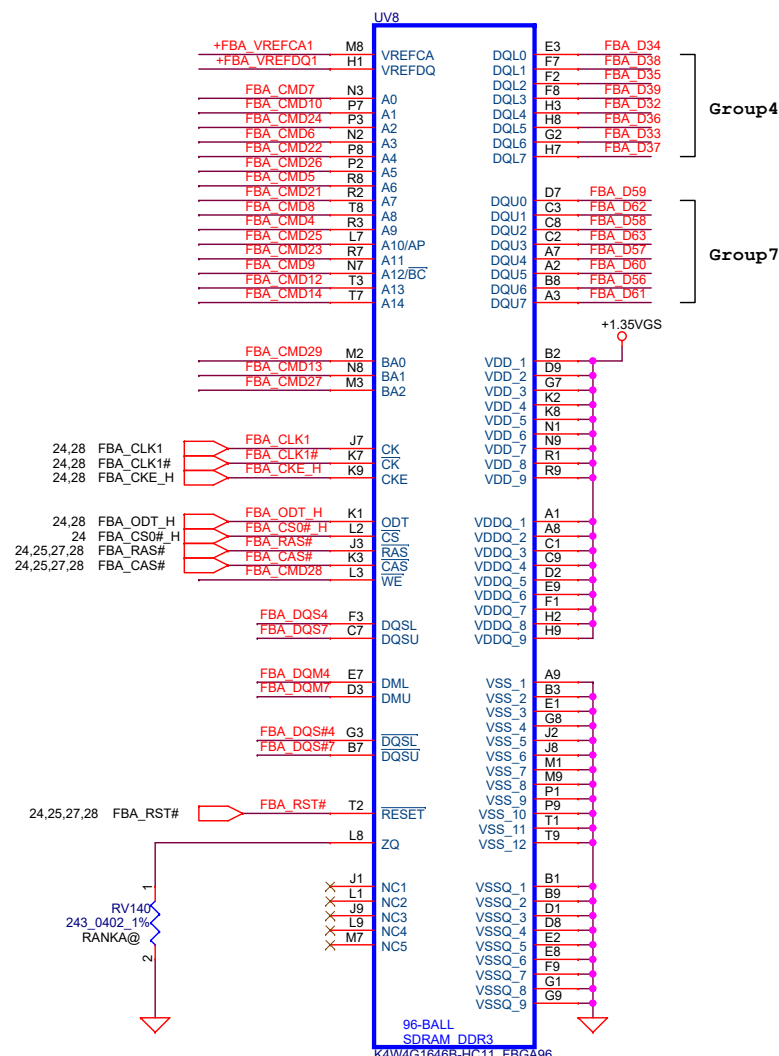
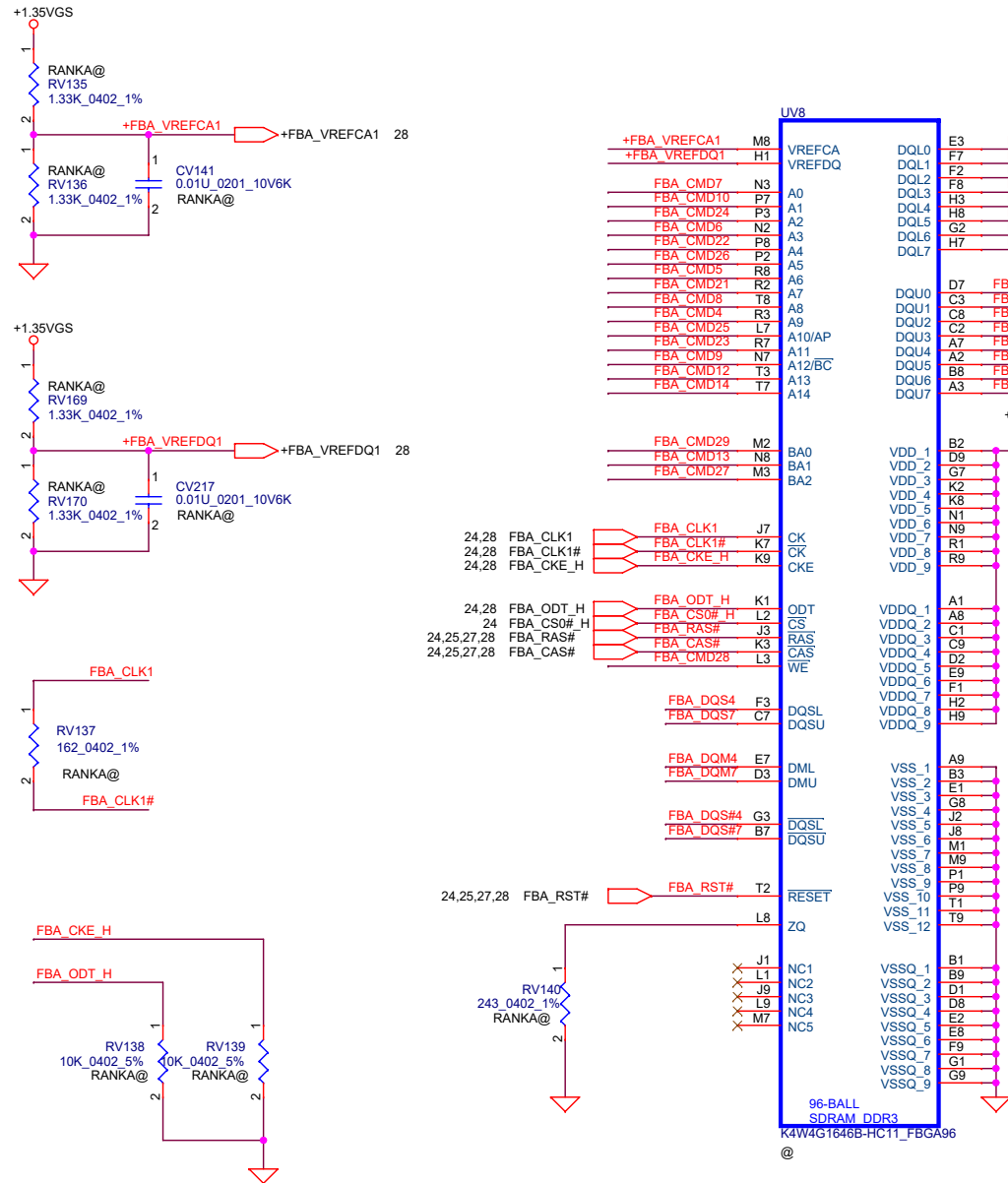


CMD mapping mod Mode E

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17			CS1#_H	
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2



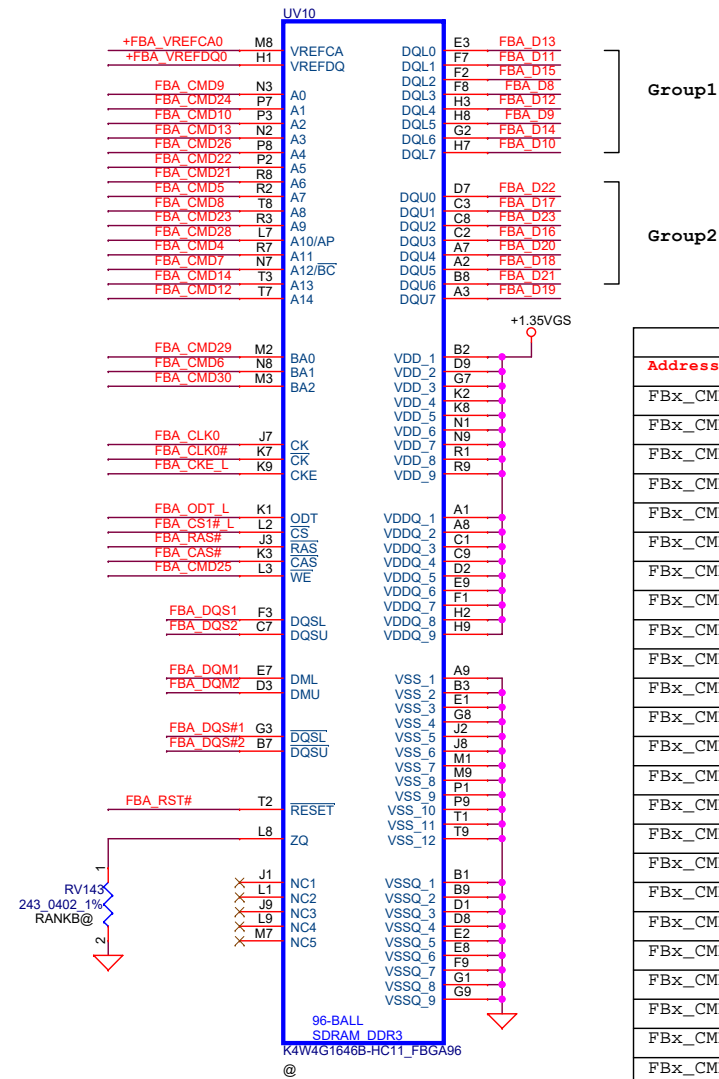
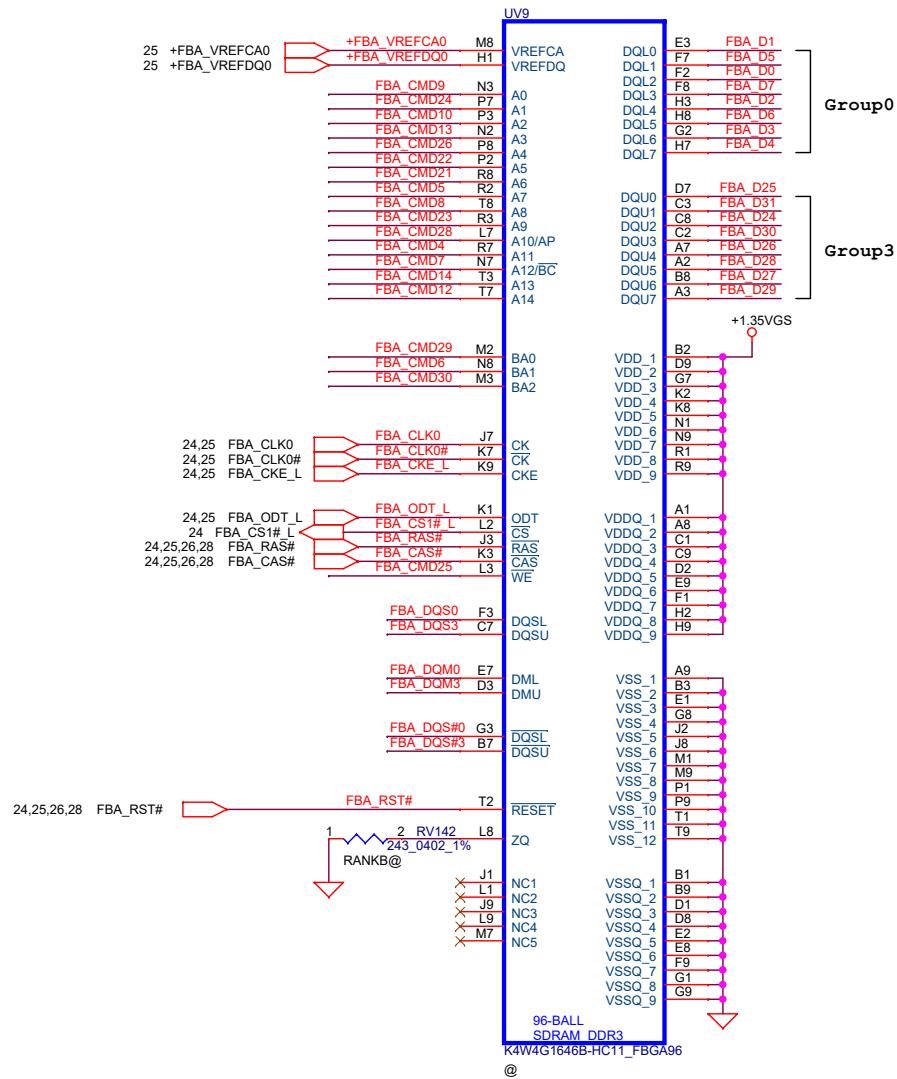
at least 16 mils width(optimal)
20 mils spacing to other signals /planes



CMD mapping mod Mode E

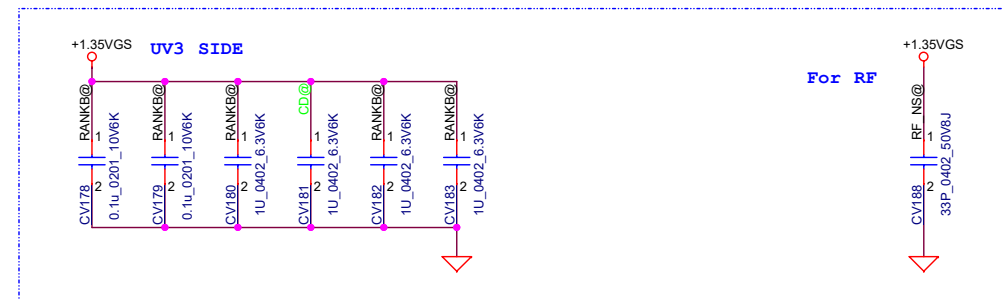
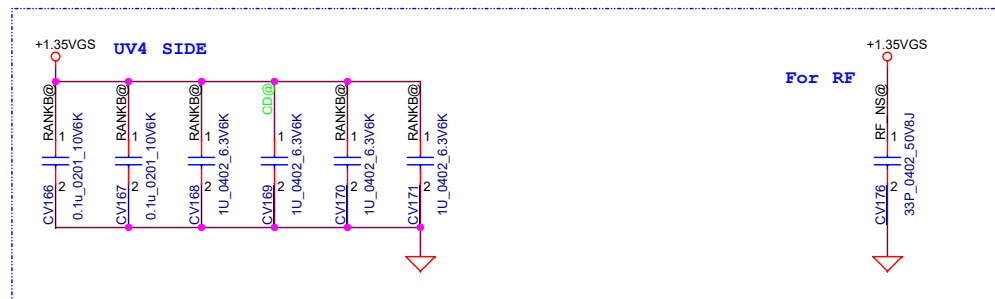
Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17			CS1#_H	
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2

at least 16 mils width(optimal)
20 mils spacing to other signals /planes

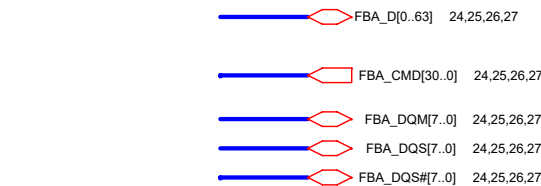
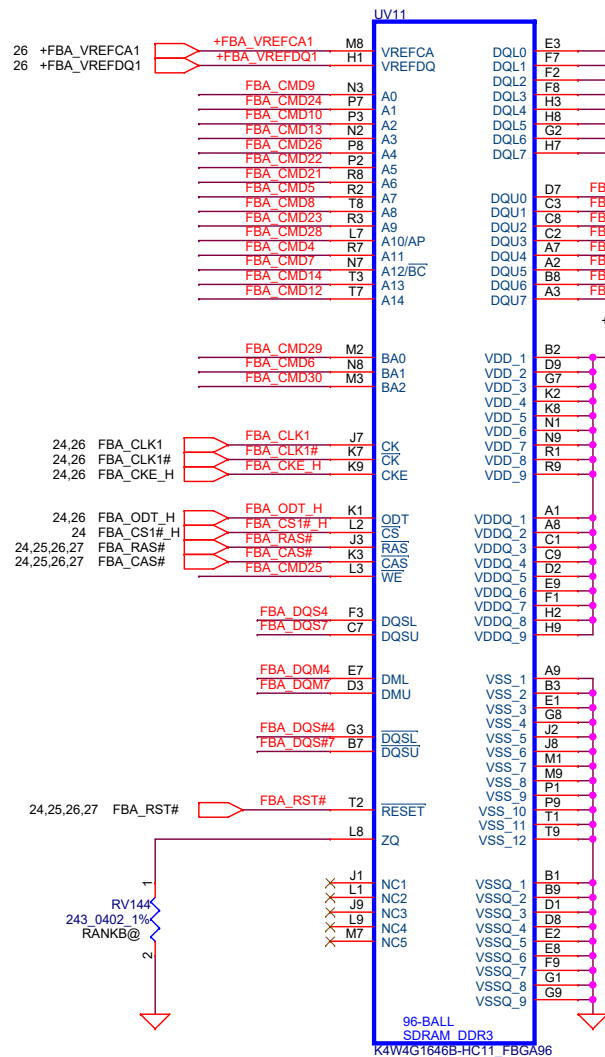


CMD mapping mod Mode E

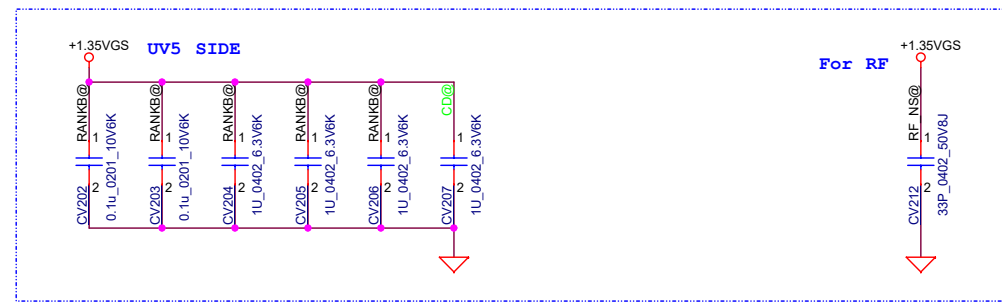
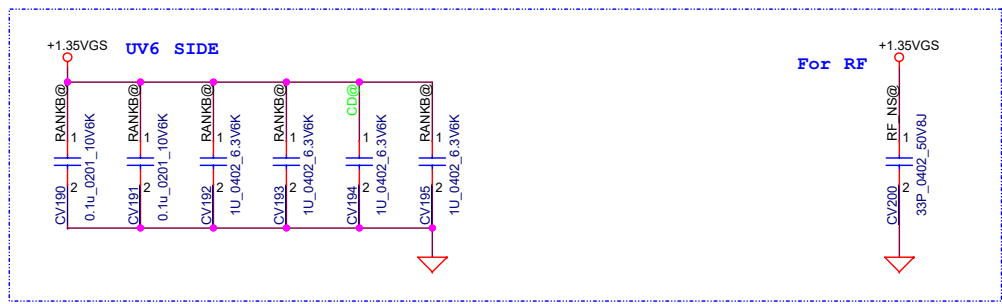
Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17			CS1#_H	
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2

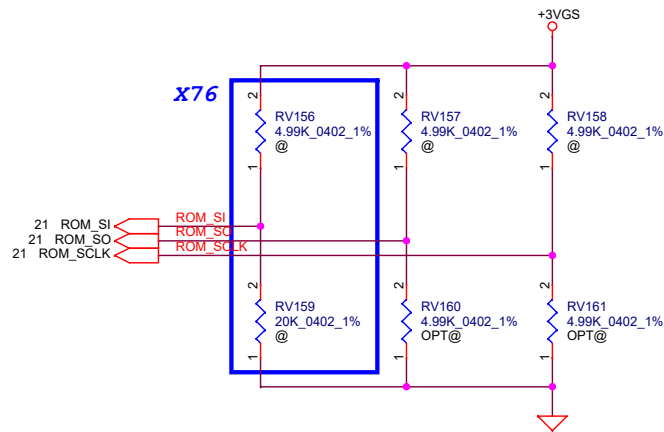
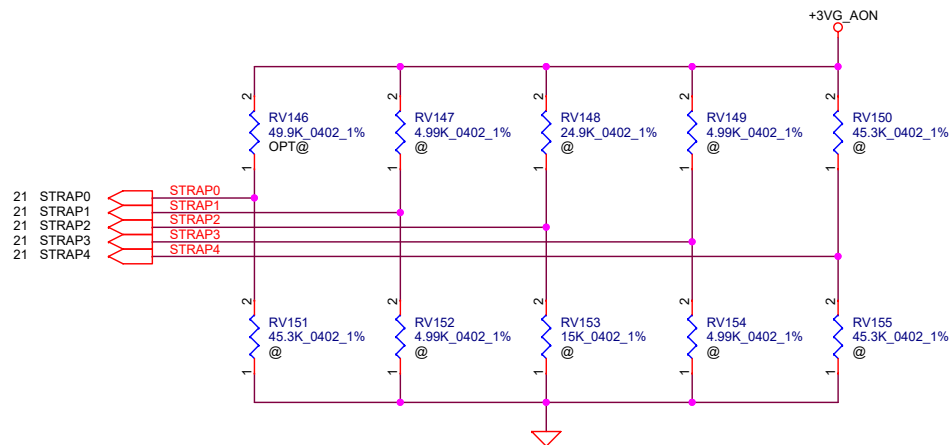


at least 16 mils width(optional)
20 mils spacing to other signals /planes



CMD mapping mod Mode E				
Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17			CS1#_H	
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

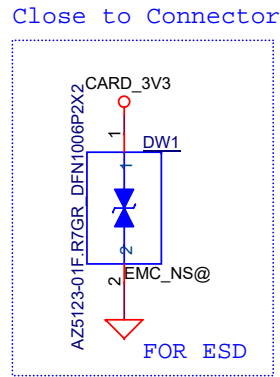
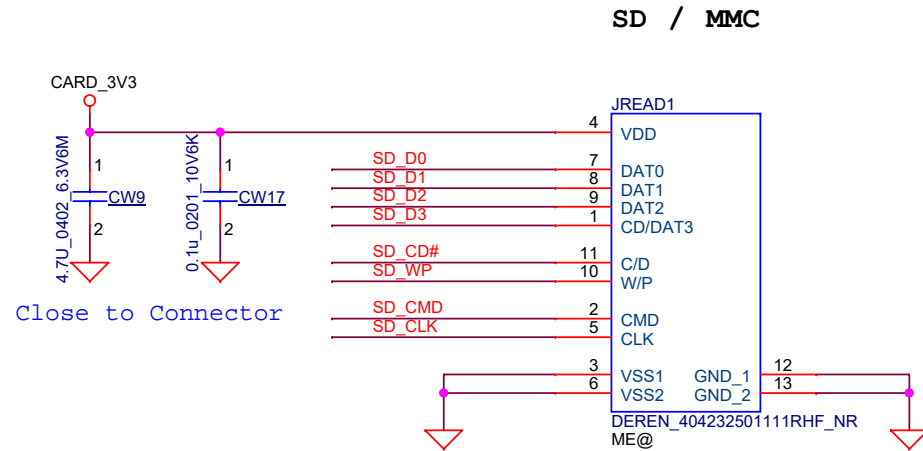
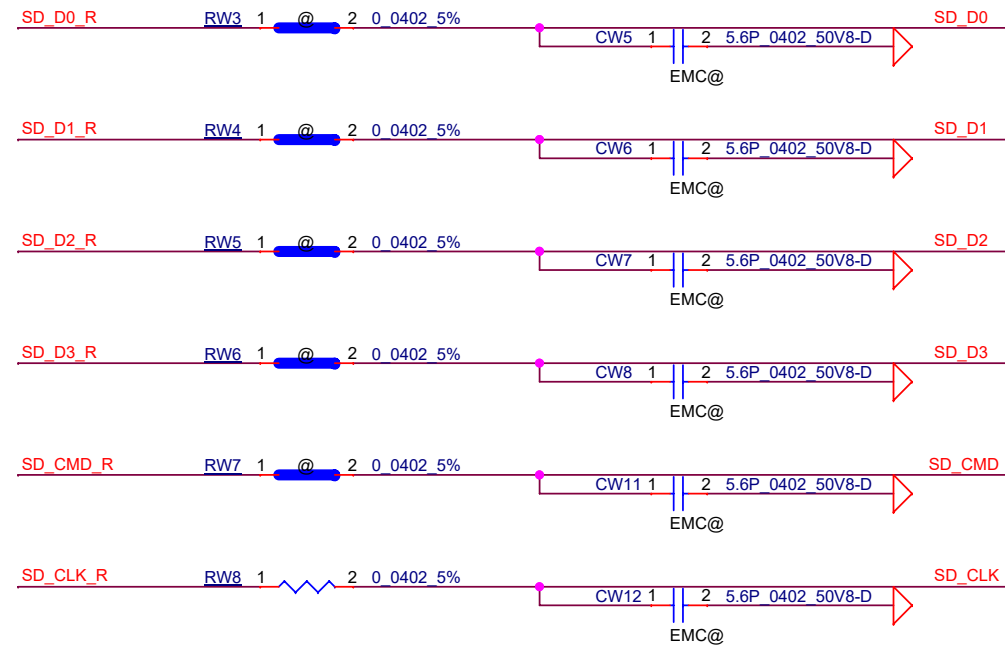
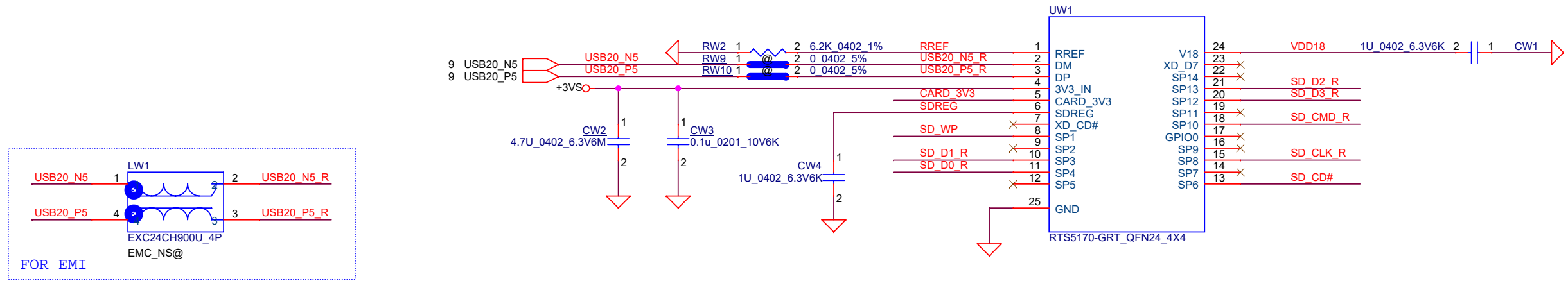
PCIE_CFG	
0	(Default)
1	


SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

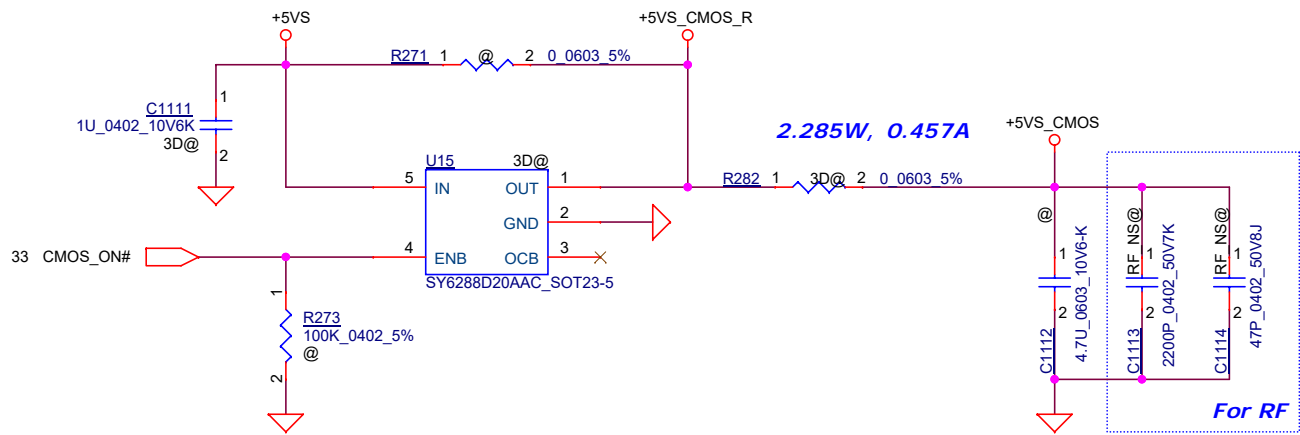
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

GPU	Configuration	FB Memory (DDR3L)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR N16V-GMR1	Single-Rank	Samsung 900MHz	K4W4G1646E-BC1A 256M x 16	0x1 PD 10K	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
		Hynix 900MHz	H5TC4G63CFR-N0C 256M x 16	0x2 PD 15K							
		Micron 900MHz	MT41J256M16LY-091G:N	0x6							
			256M x 16	PD 34.8K							
	Dual-Rank	Samsung 900MHz	K4W4G1646E-BC1A 256M x 16	0xF PU 45.3K							
		Hynix 900MHz	H5TC4G63CFR-N0C 256M x 16	0xE PU 34.8K							
		Micron 900MHz	MT41J256M16LY-091G:N	0xA							
			256M x 16	PU 15K							

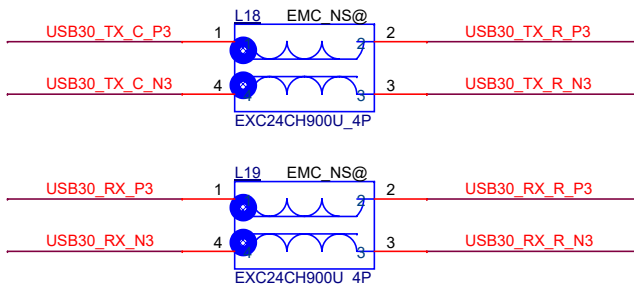
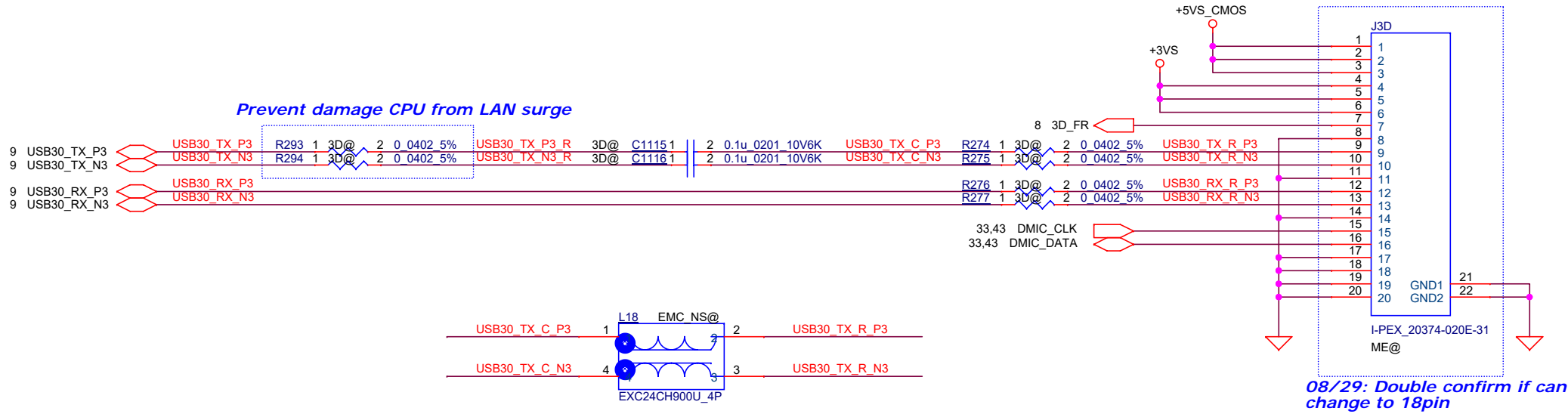
VRAM	X76 P/N	VRAM Q'ty	VRAM P/N
Samsung	X7610212201	4	SA000063F20
	X7610212001	8	
Hynix	X7610212202	4	SA00007DU10
	X7610212101	8	
Micron	X7610212203	4	SA00007QJ00
	N/A	8	




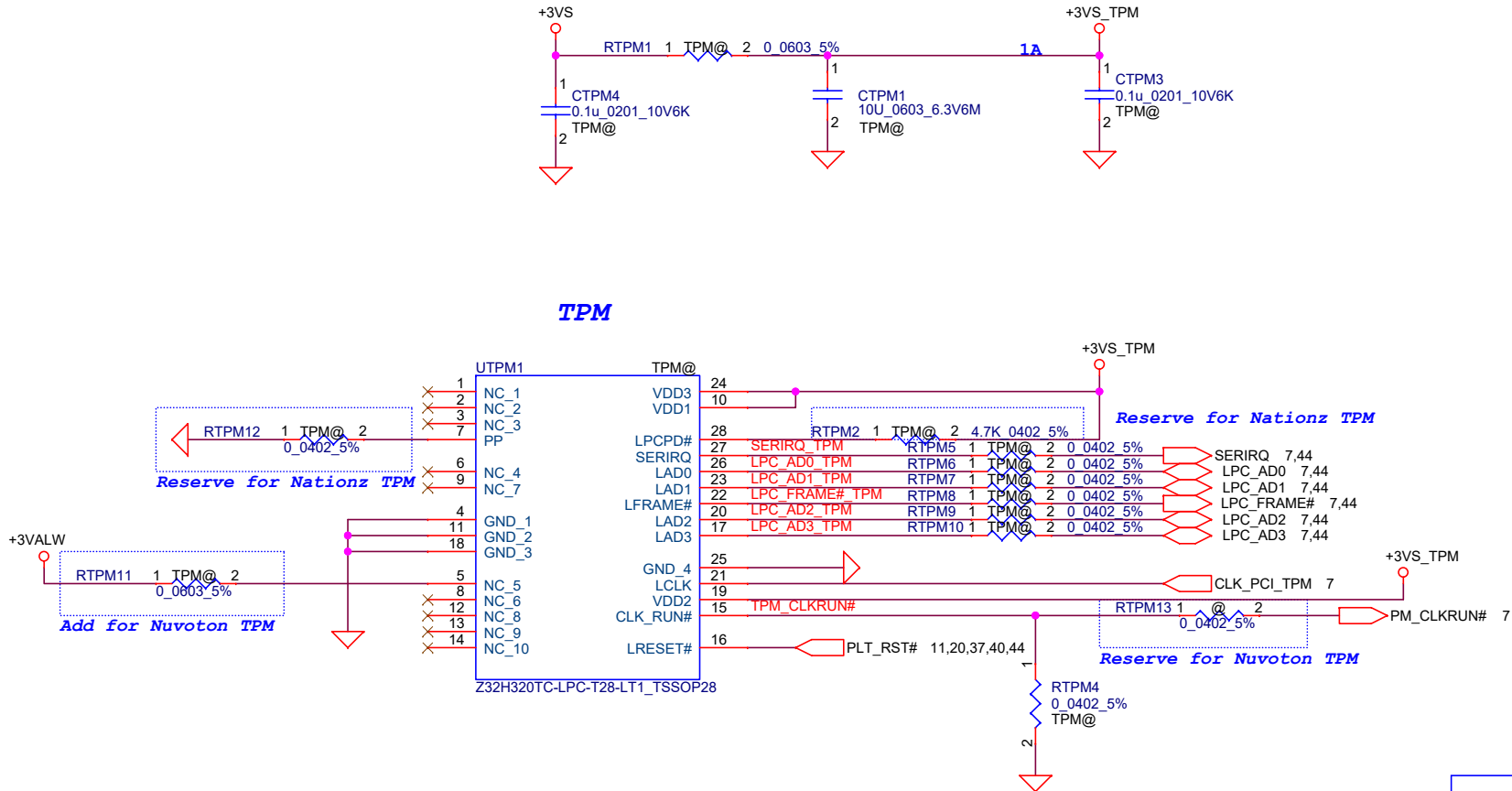
Security Classification		LC Future Center Secret Data		Title Cardreader					
Issued Date		2015/08/20						Deciphered Date	
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Size Custom		Document Number CG411						Rev 1.0	
Date:		Thursday, January 14, 2016				Sheet 30 of 60			




3D Camera DB Connector



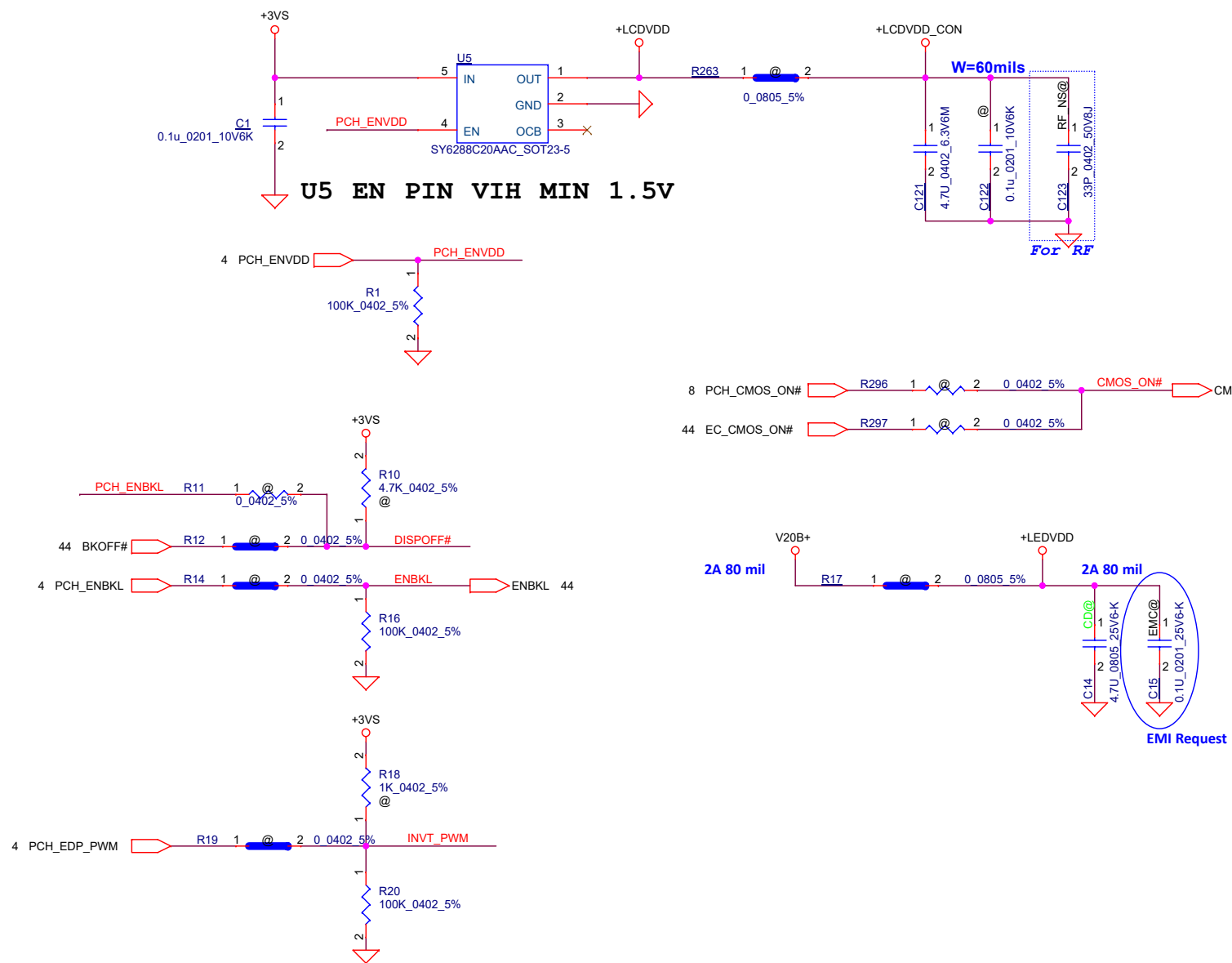
Security Classification		LC Future Center Secret Data				Title															
Issued Date		2015/08/20		Deciphered Date		2016/08/20		3D Camera													
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										Custom	CG411			1.0							
										Date:				Thursday, January 14, 2016				Sheet	31	of	60
										3				2				1			



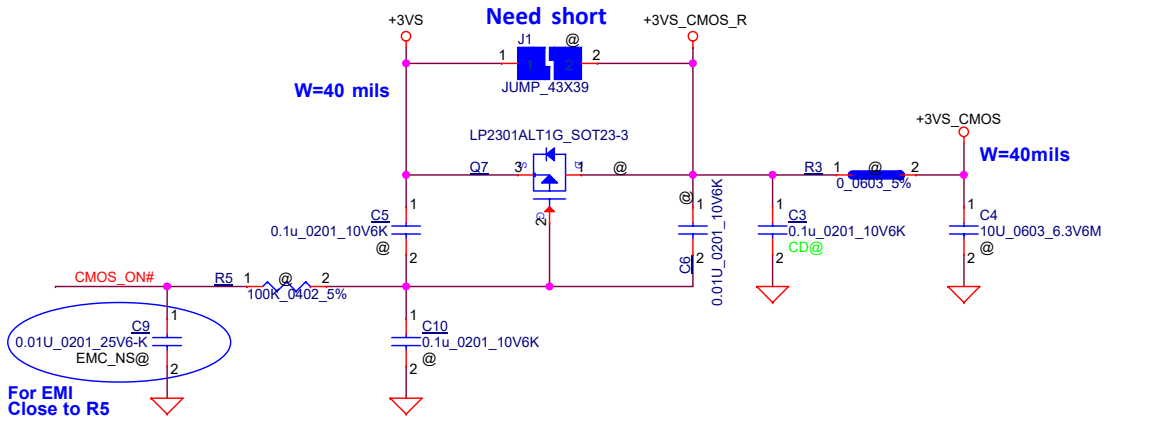
	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

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				Date: Thursday, January 14, 2016			Sheet 32 of 60
3		2		1			

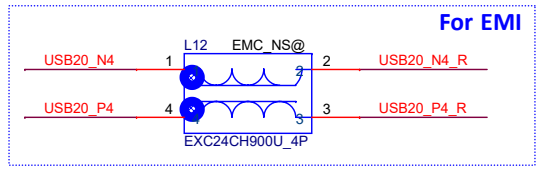
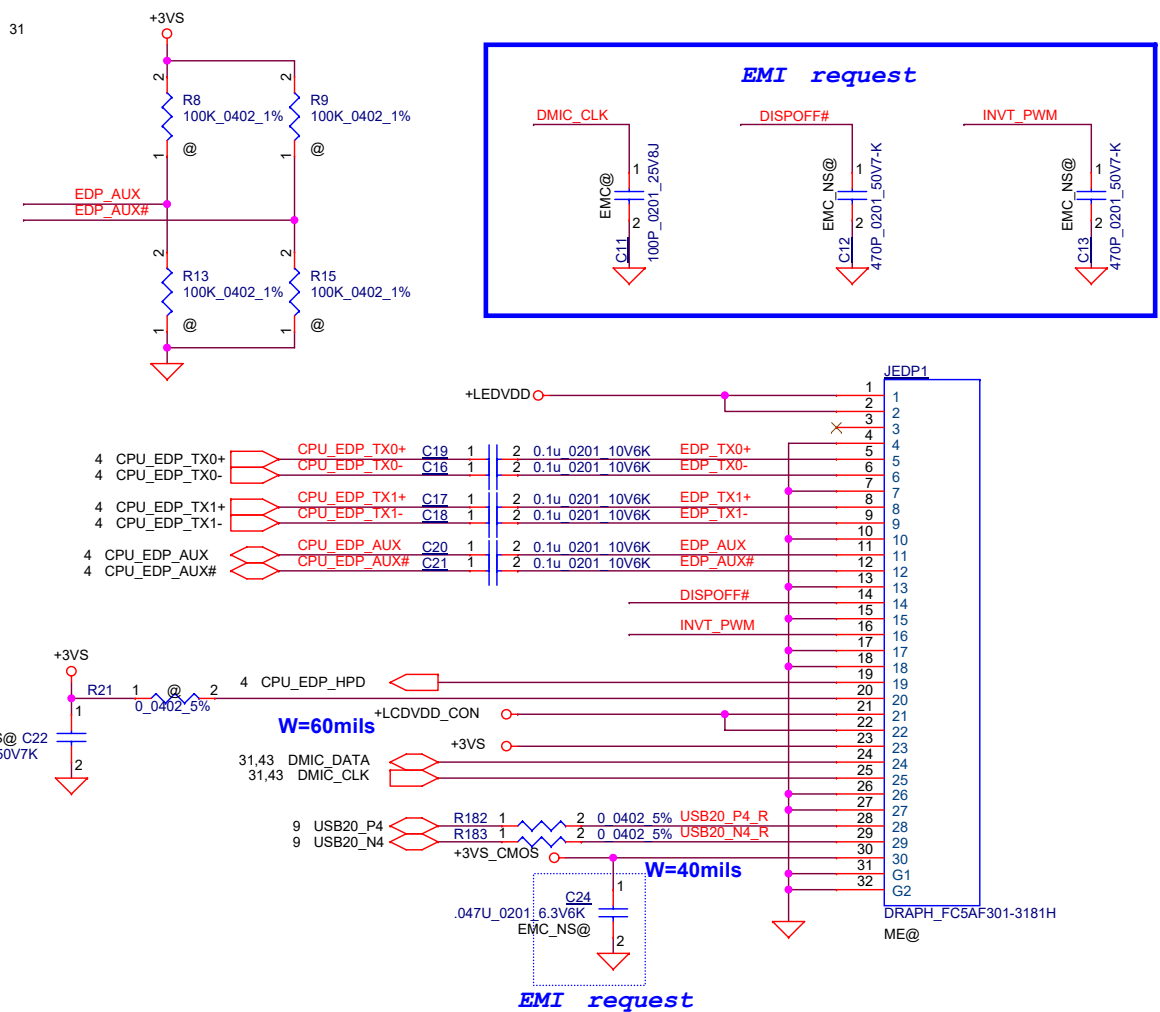
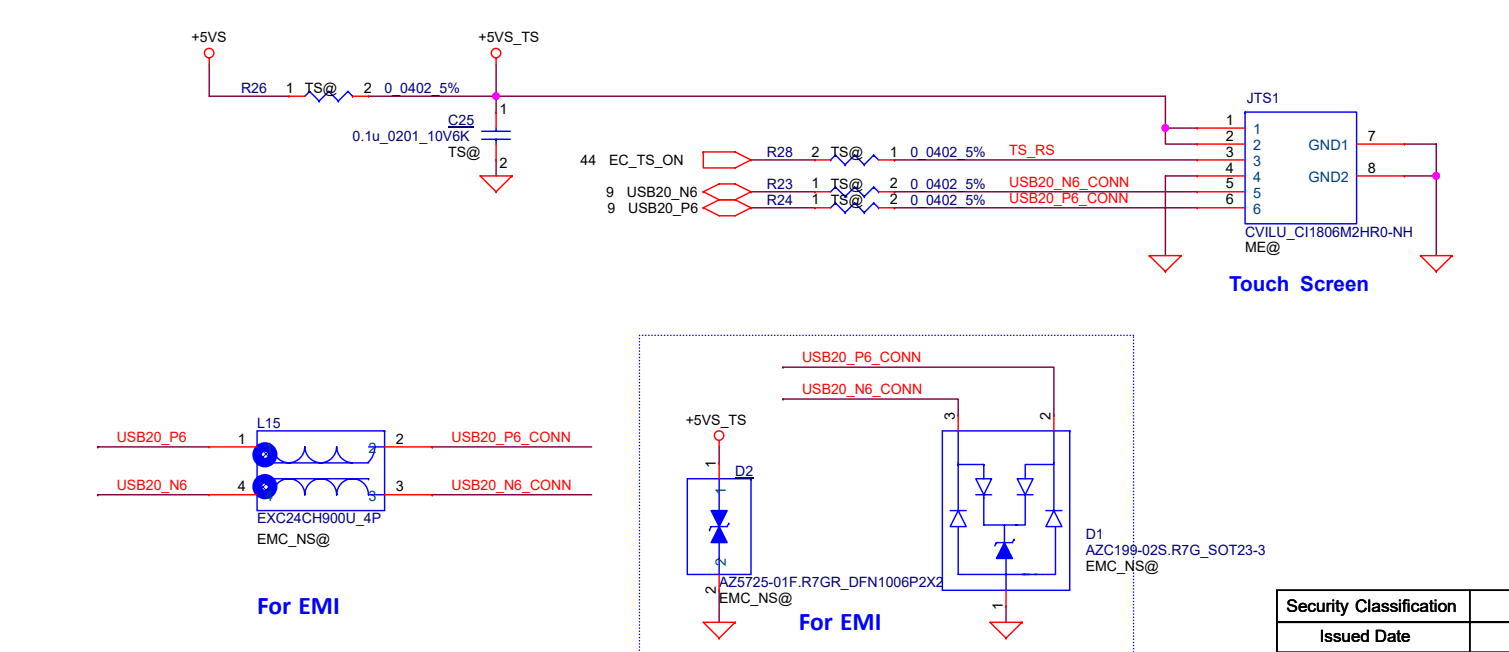
LCD POWER CIRCUIT

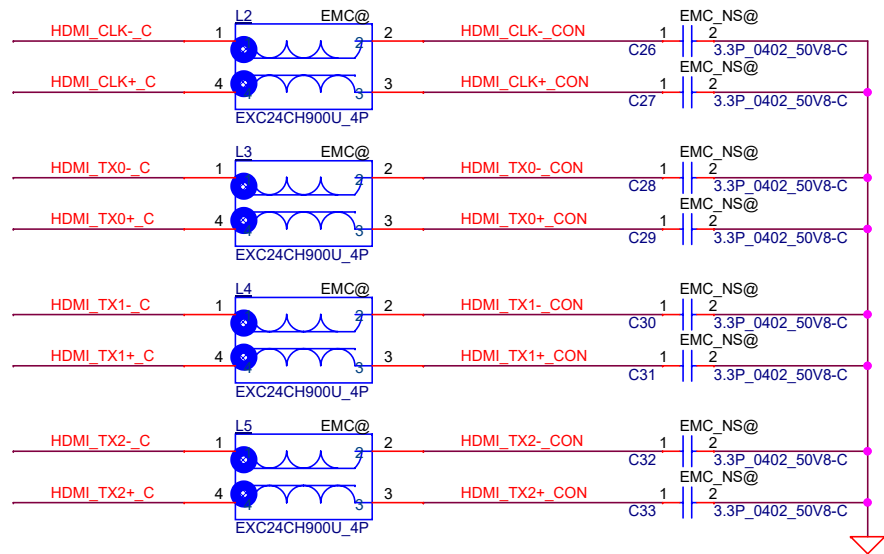


CMOS Camera

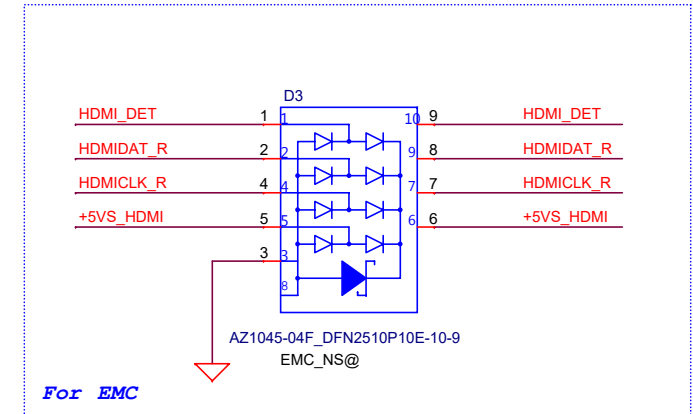
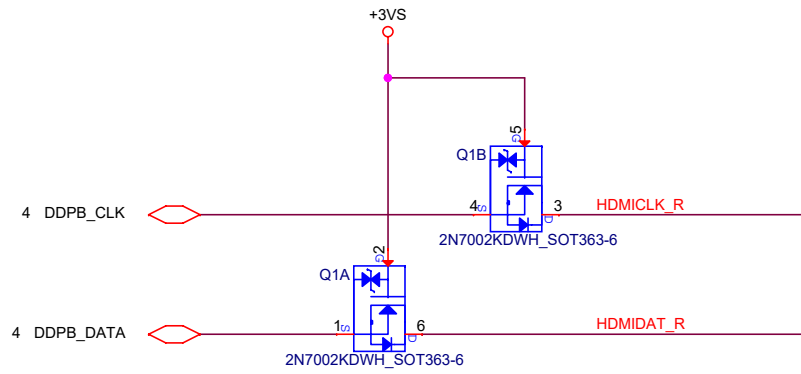
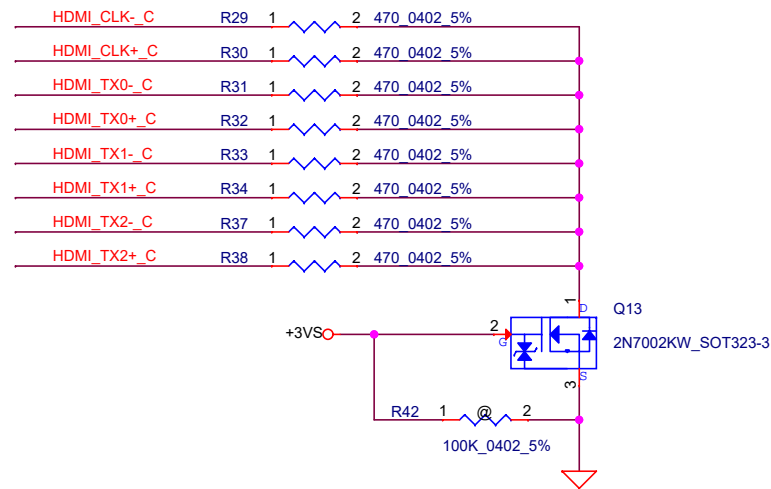


Touch Screen

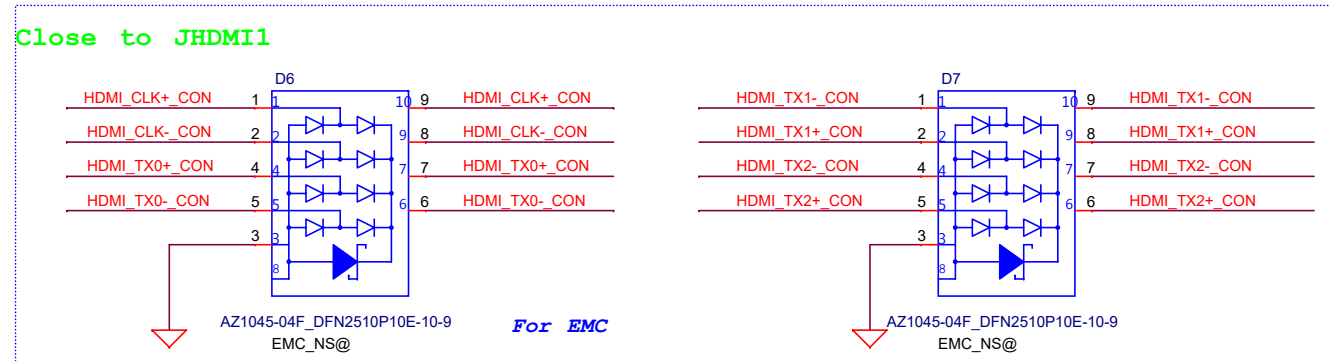
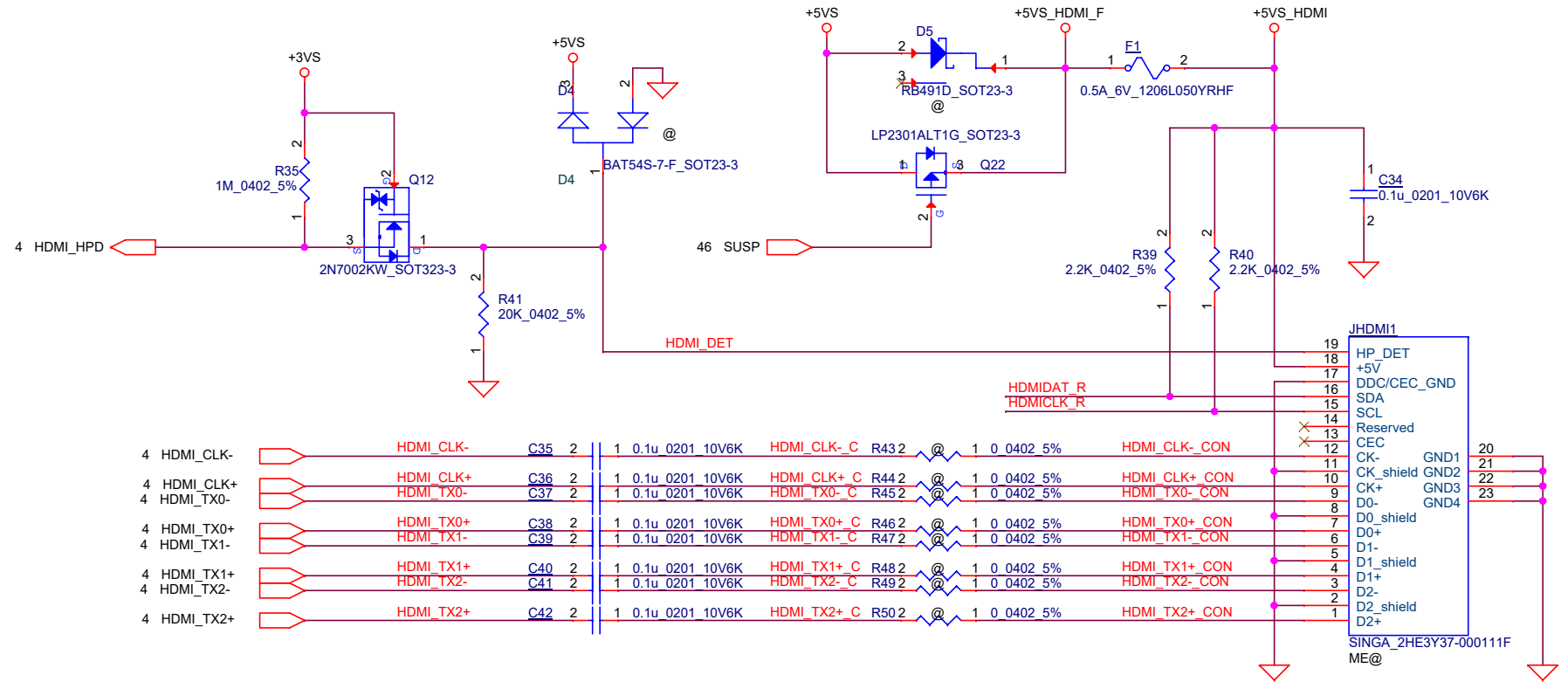




For EMC




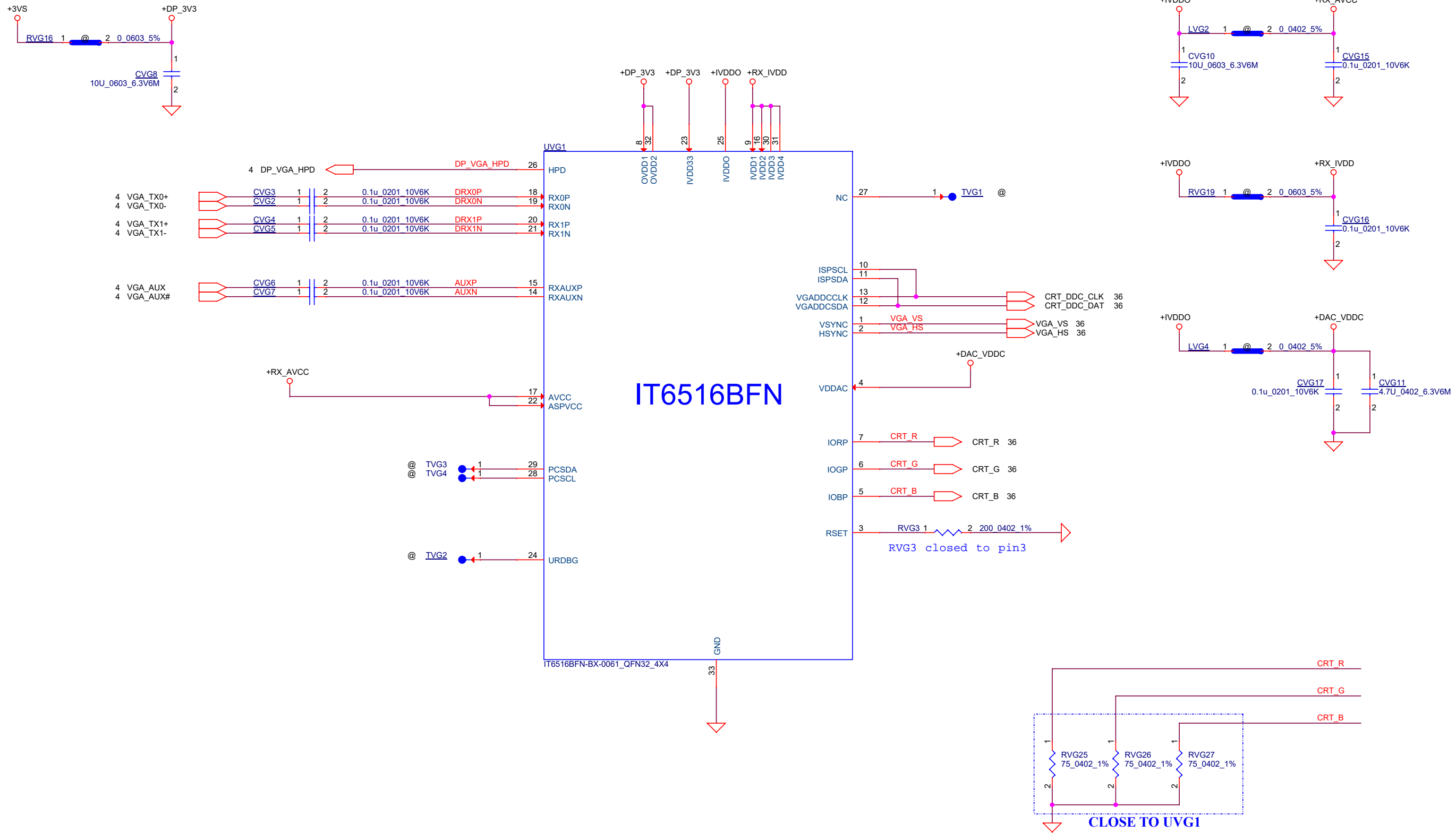
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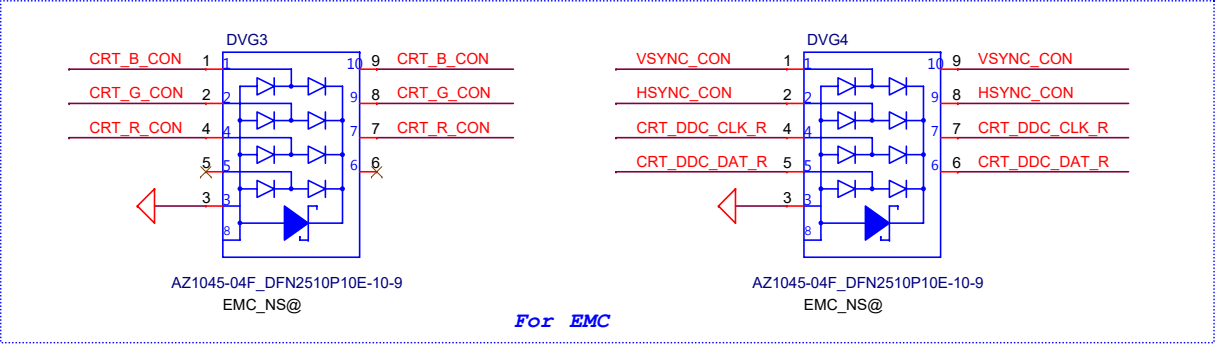
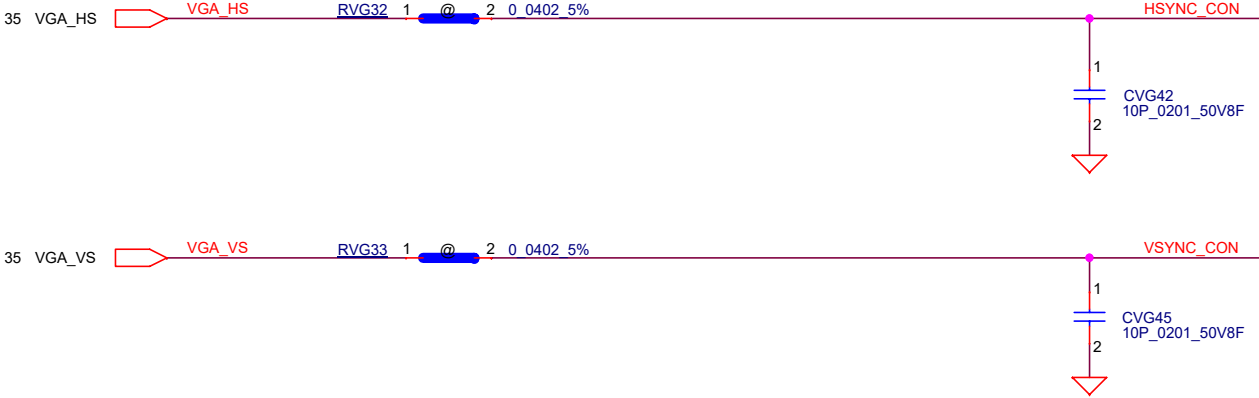
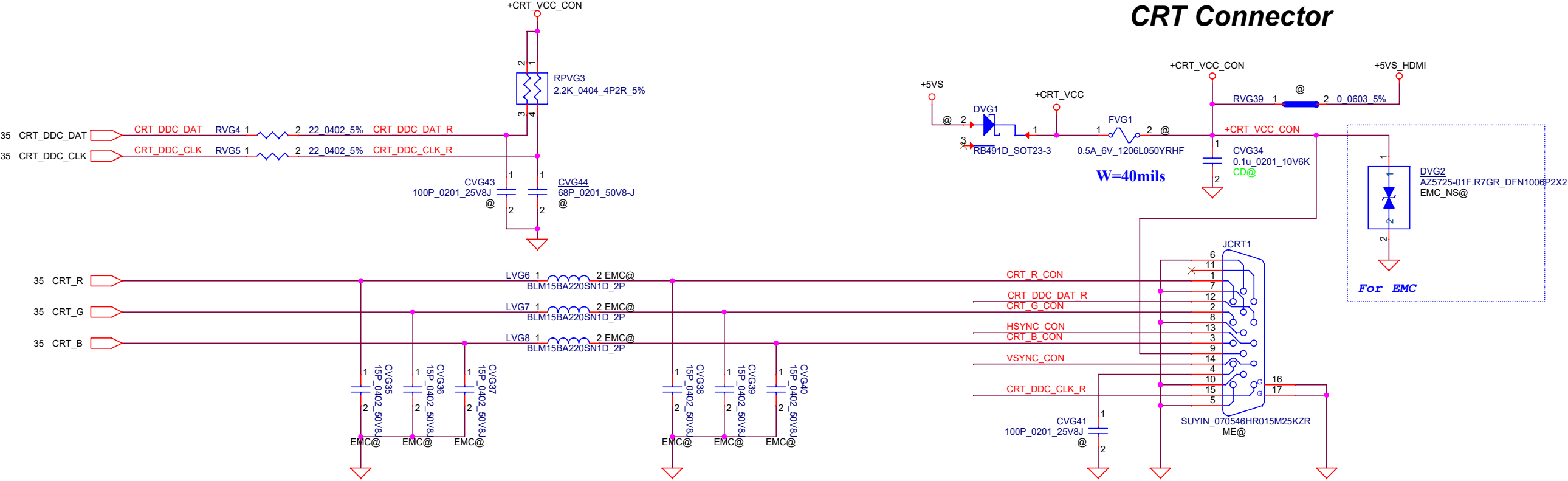
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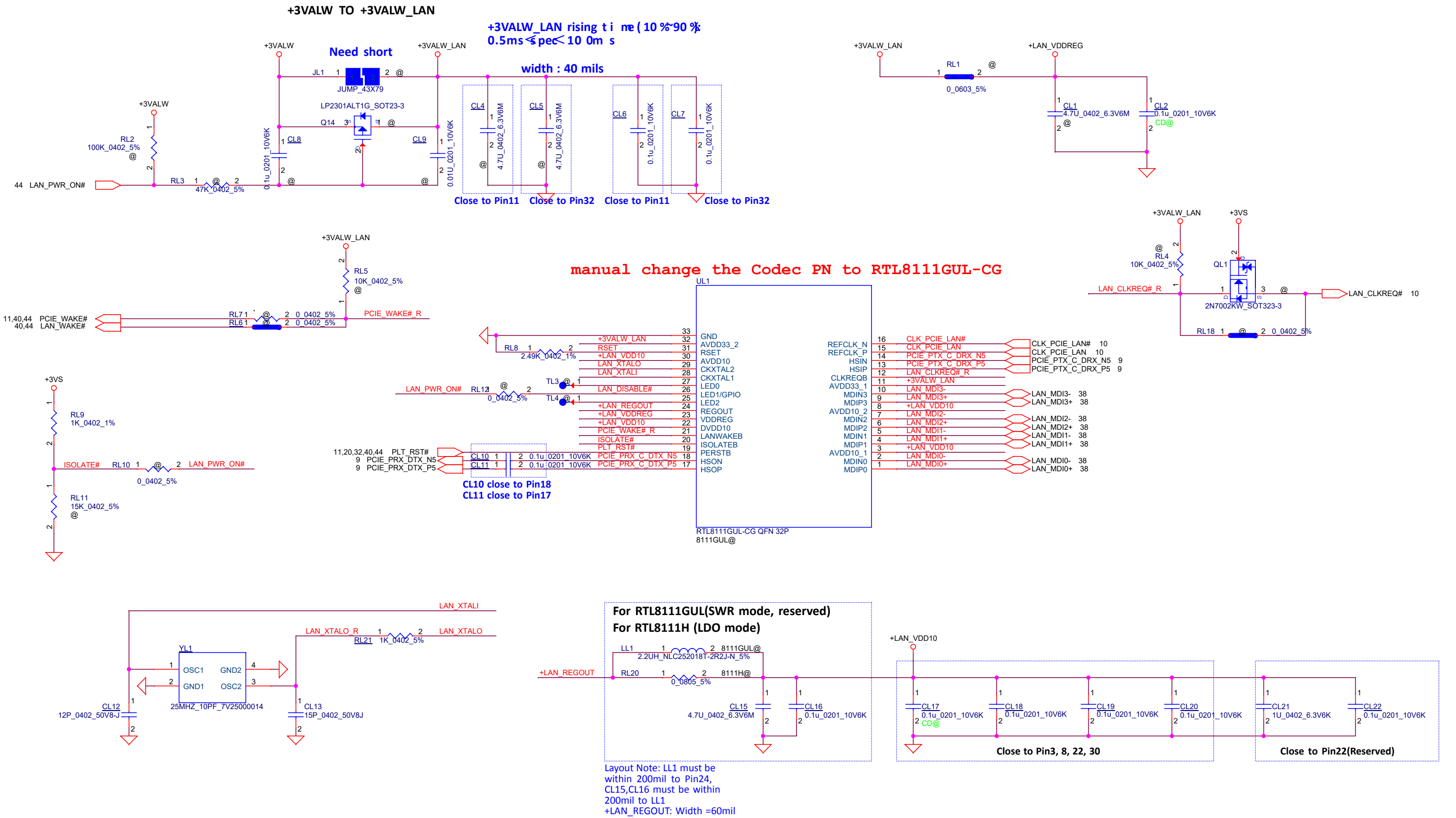
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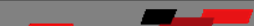
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						Size Custom		Document Number		Rev 1.0	
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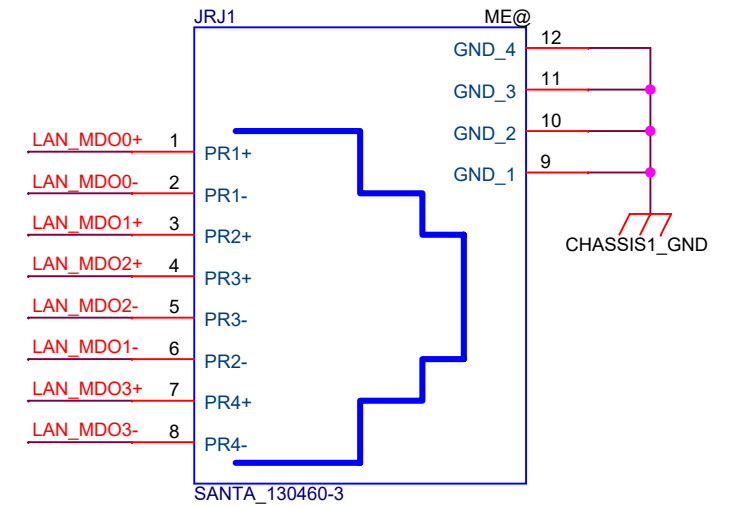
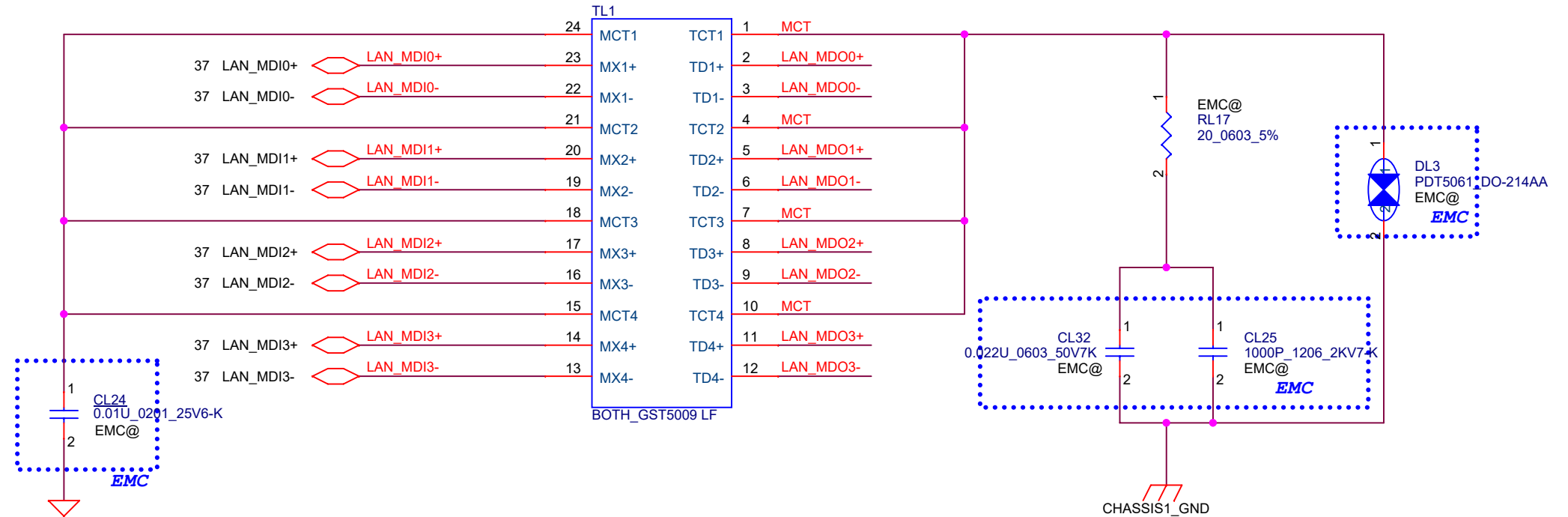
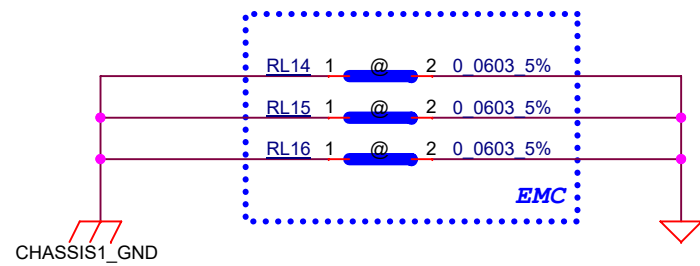
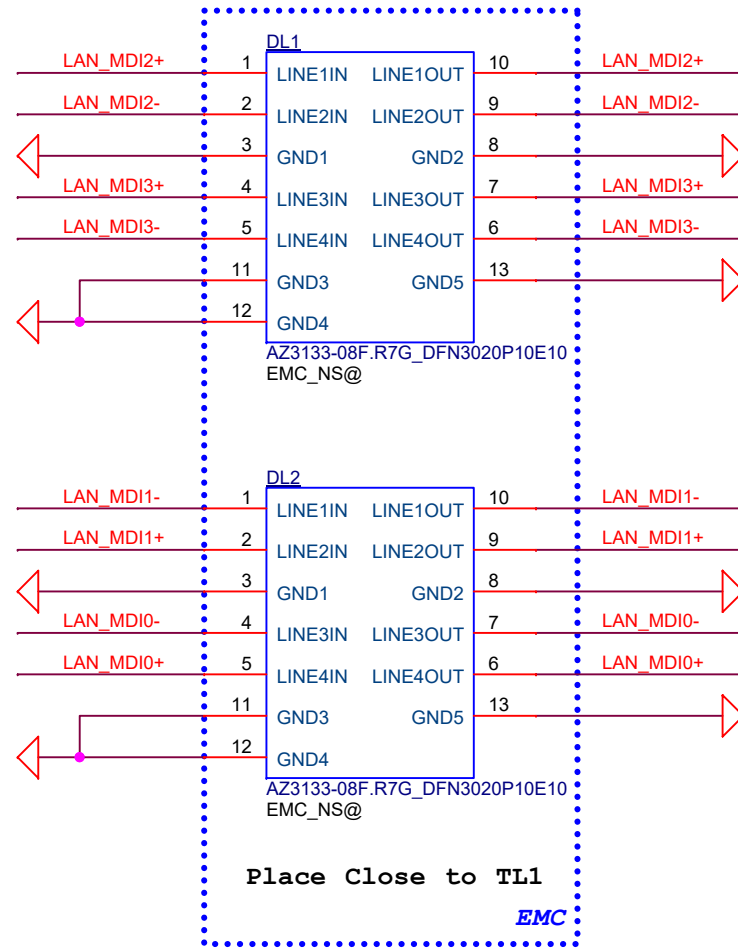
CRT Connector




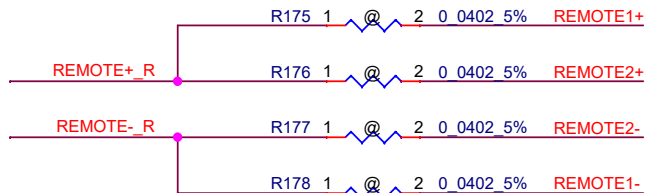
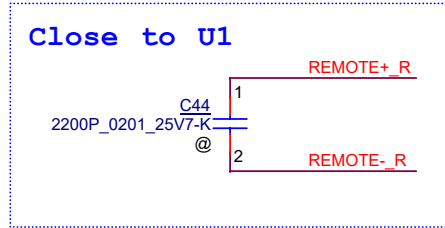


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Date: Thursday, January 14, 2016				Sheet	37	of 60

DL1/DL2
1'S PN:SC300003M00

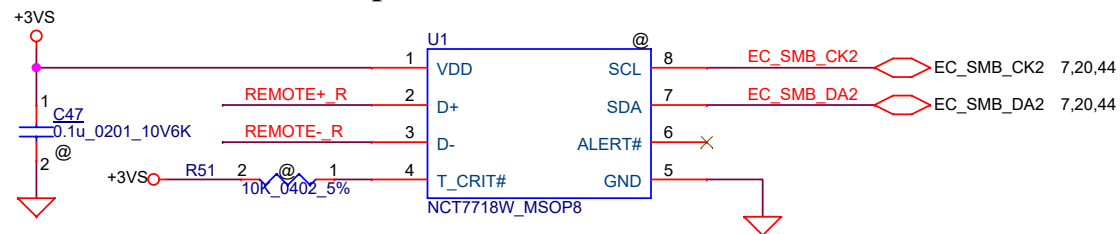


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Issued Date	2015/08/20	Deciphered Date	2016/08/20	LAN_Transformer		
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				Date: Thursday, January 14, 2016		Sheet 38 of 60

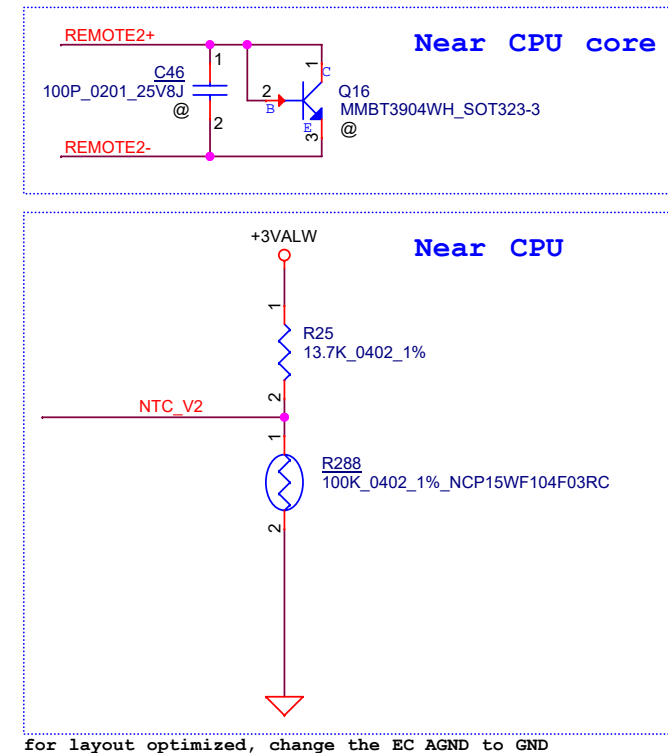
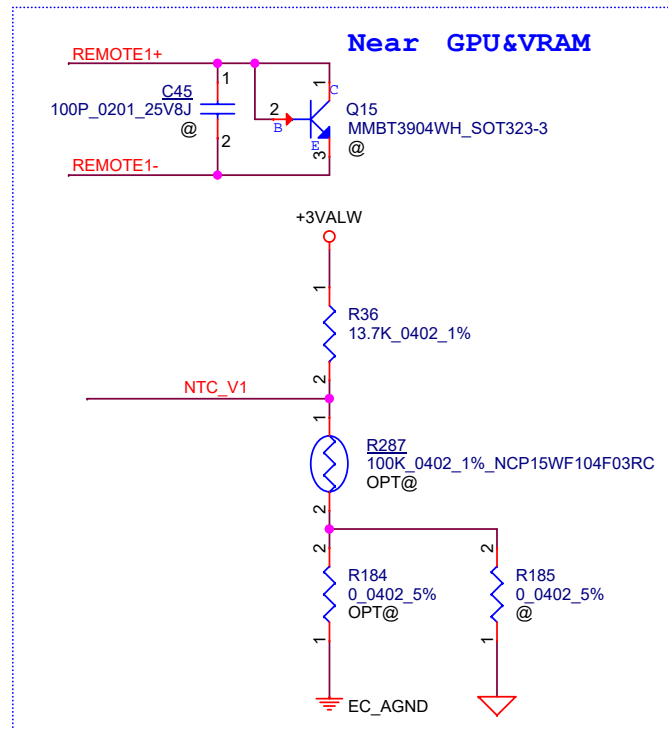


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

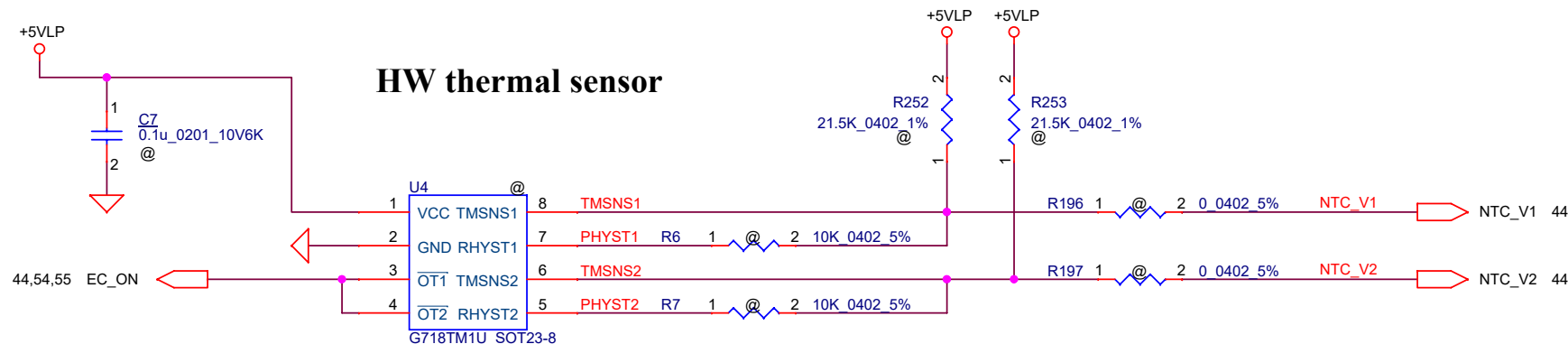
SMSC thermal sensor placed near DIMM



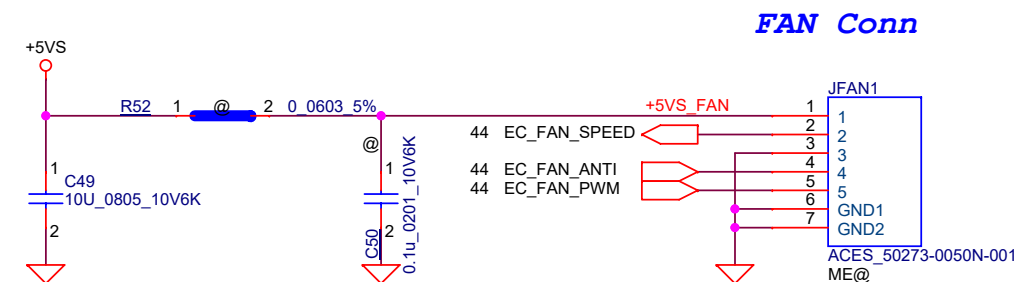
Address 1001_101xb



HW thermal sensor

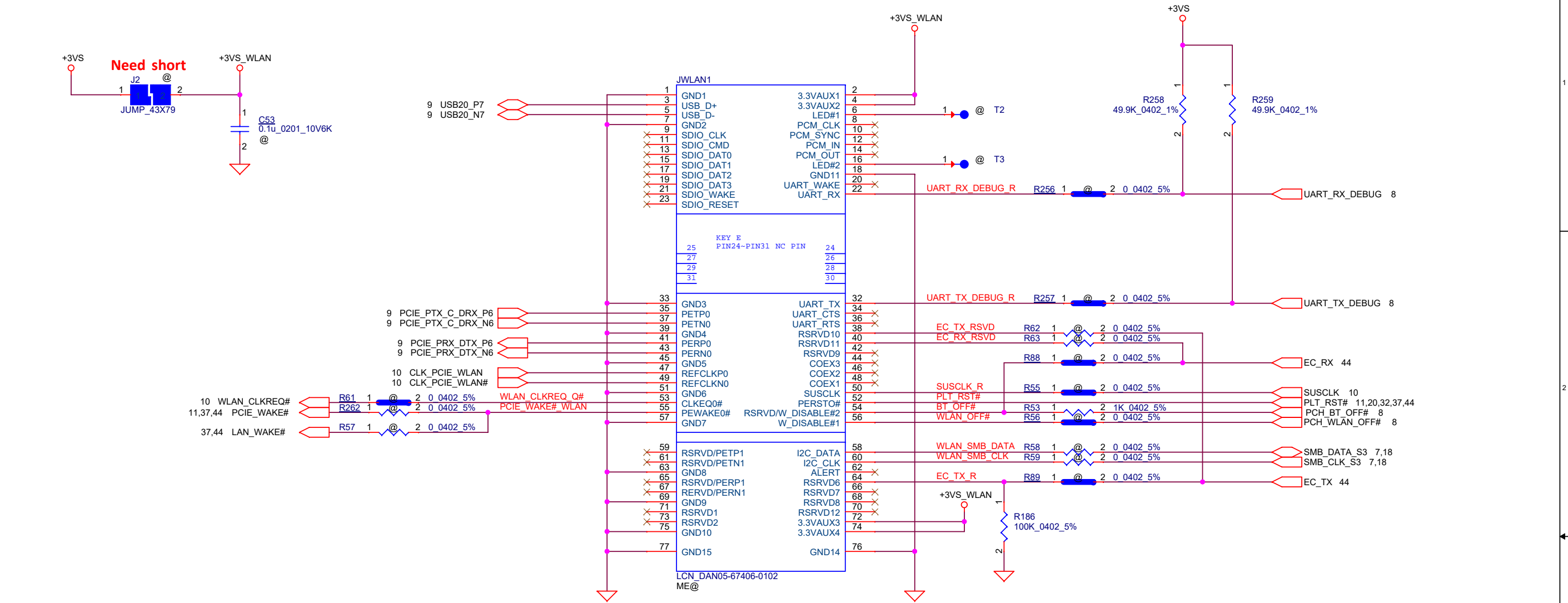


over temperature threshold:
 $RSET=3*RTMH$
92+/-30C
Hysteresis temperature threshold.
 $RHYST=(RSET*RTML)/(3*RTML-RSET)$
56+/-30C

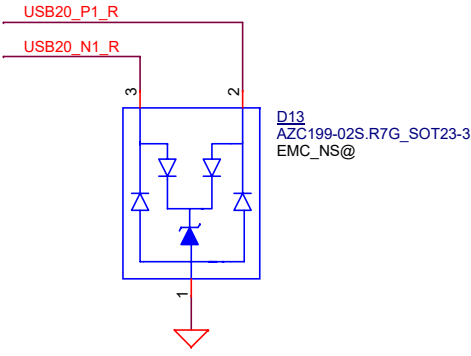
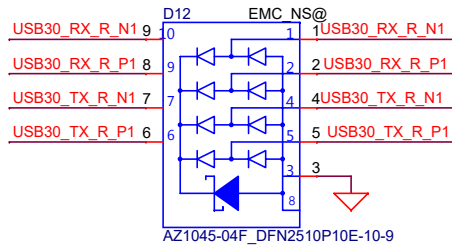
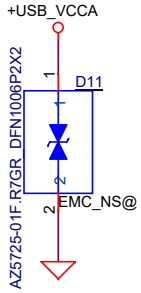
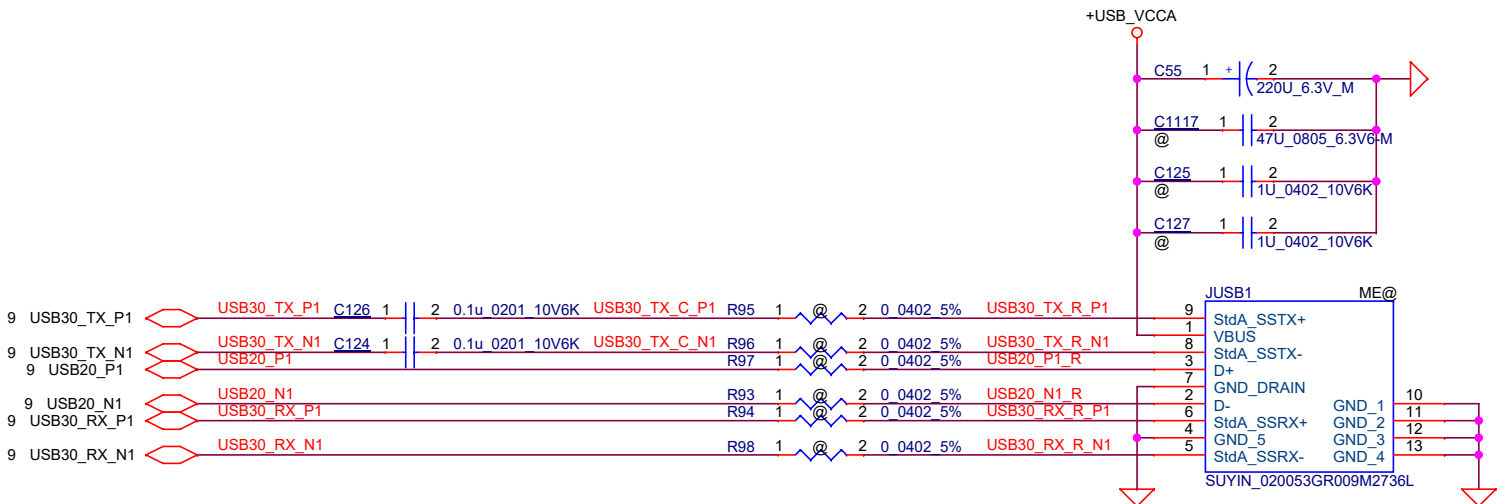
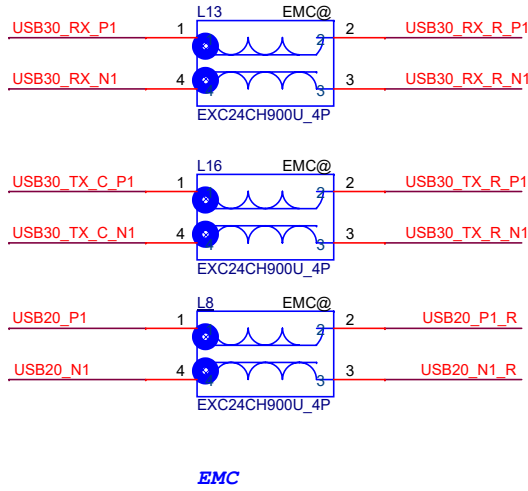
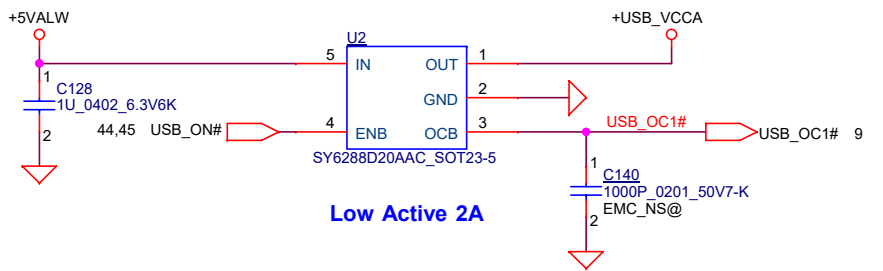


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				Date:	Thursday, January 14, 2016
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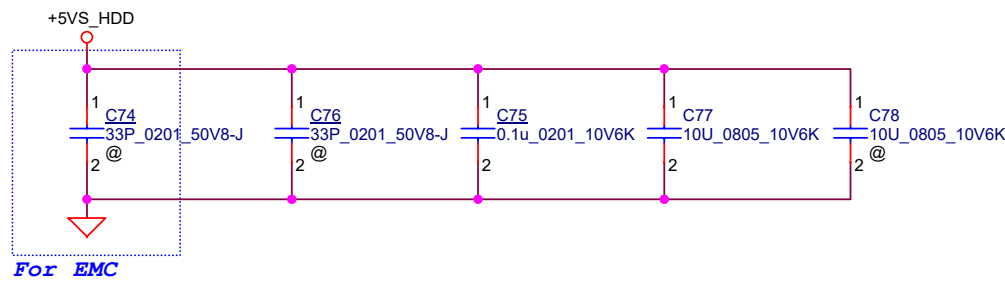
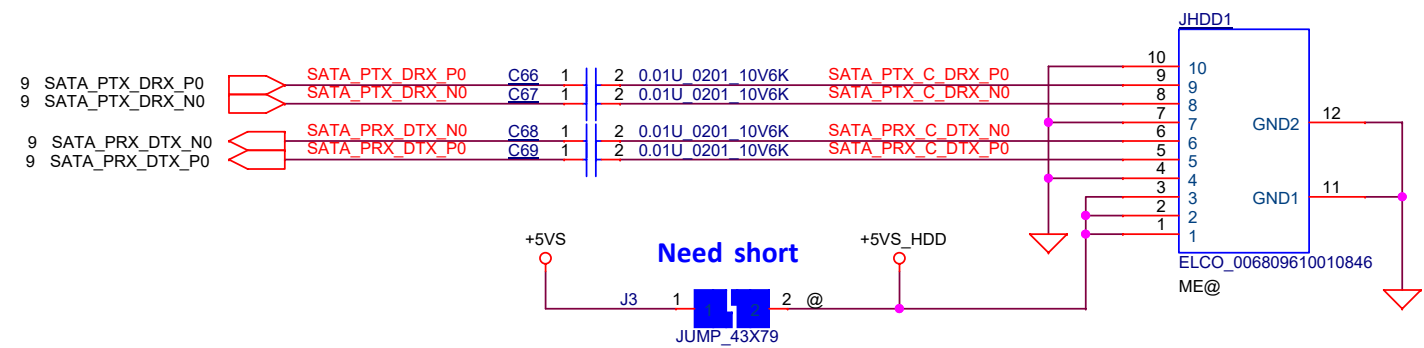
Mini-Express Card(WLAN/WiMAX)



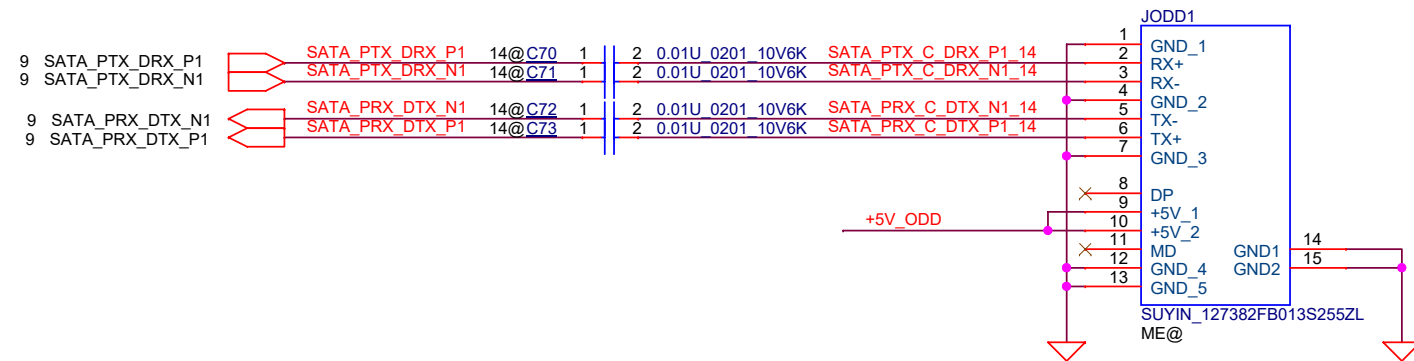
LEFT SIDE USB3.0 PORT x1



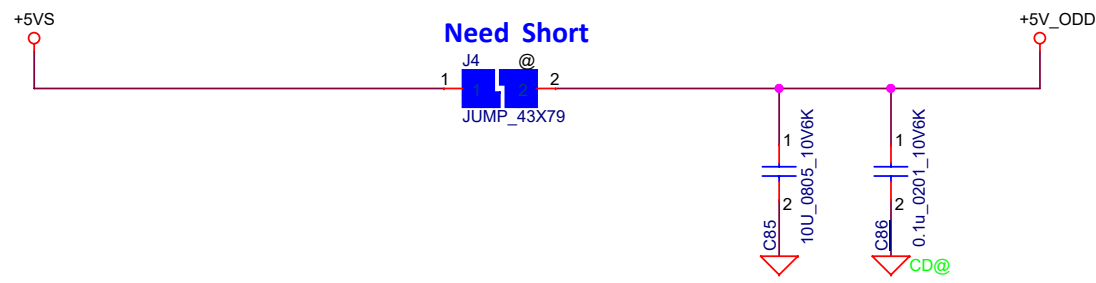
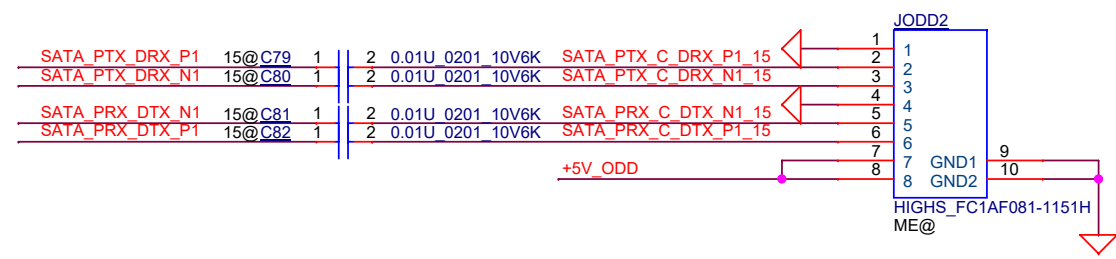
SATA HDD Conn.

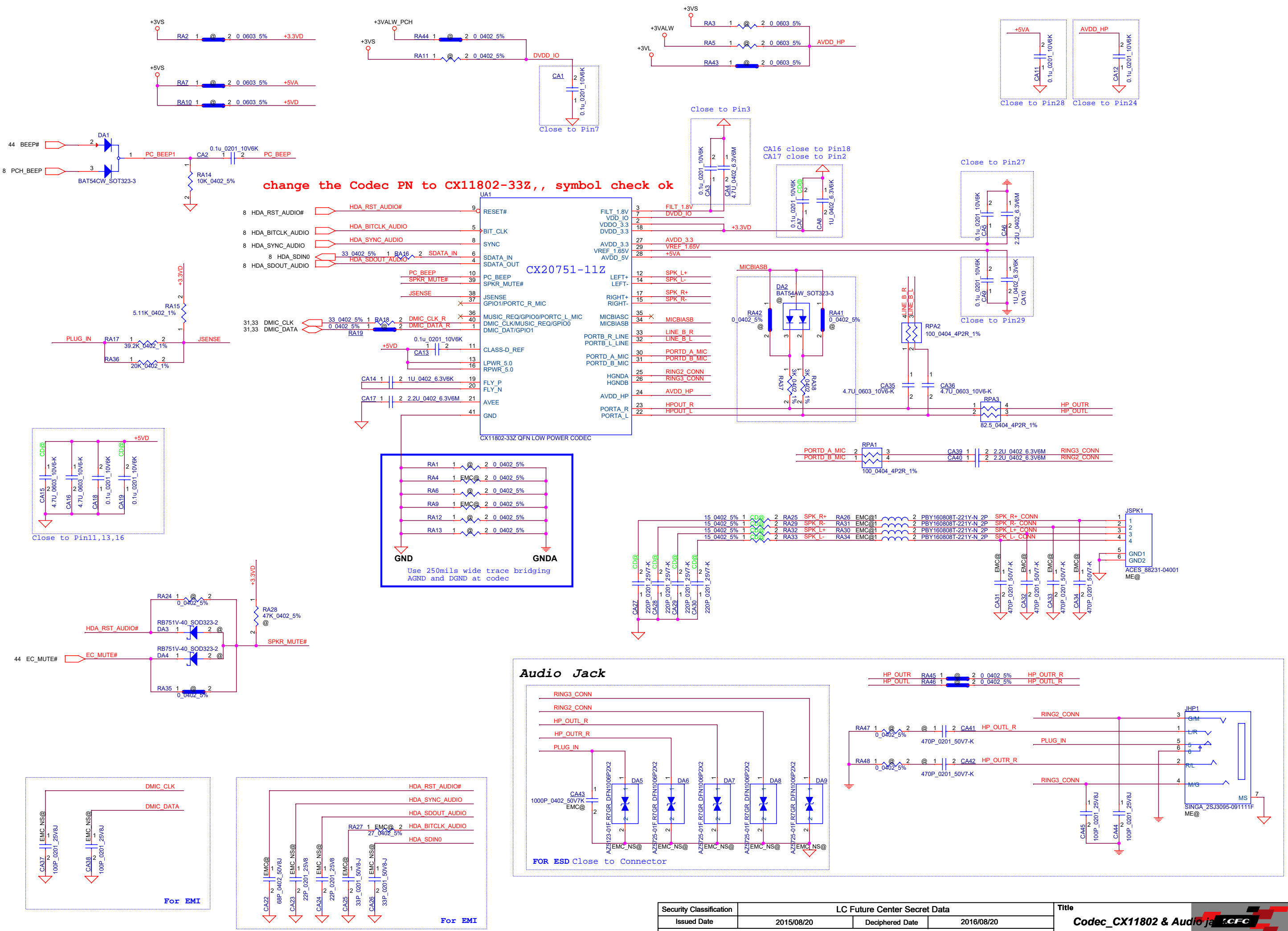


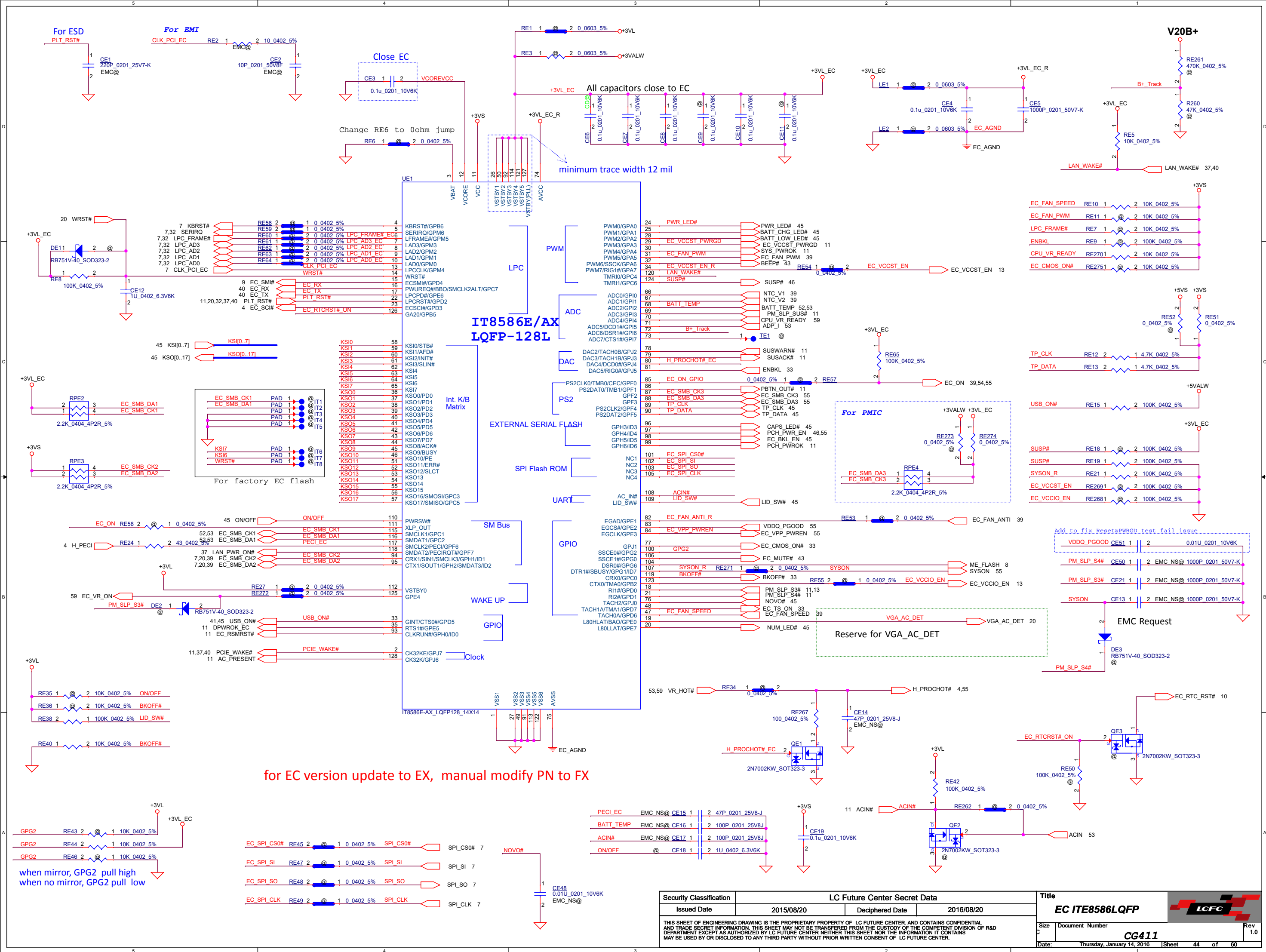
FOR 14" SATA ODD Conn.



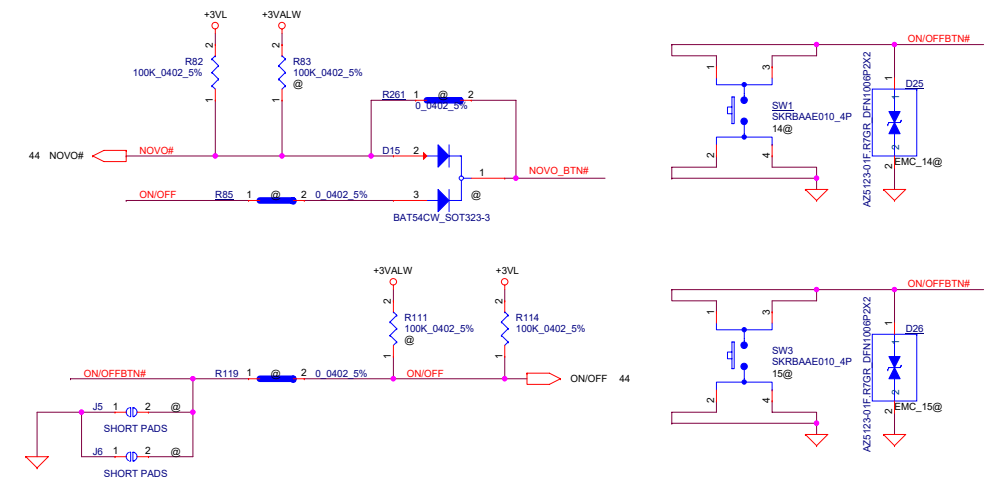
FOR 15" SATA ODD FFC Conn



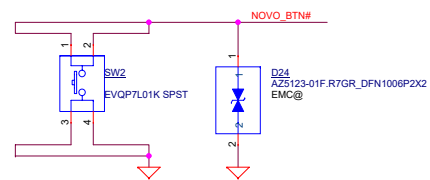




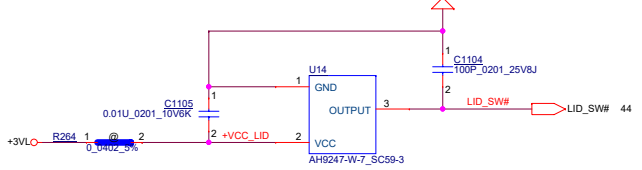
ON/OFF switch



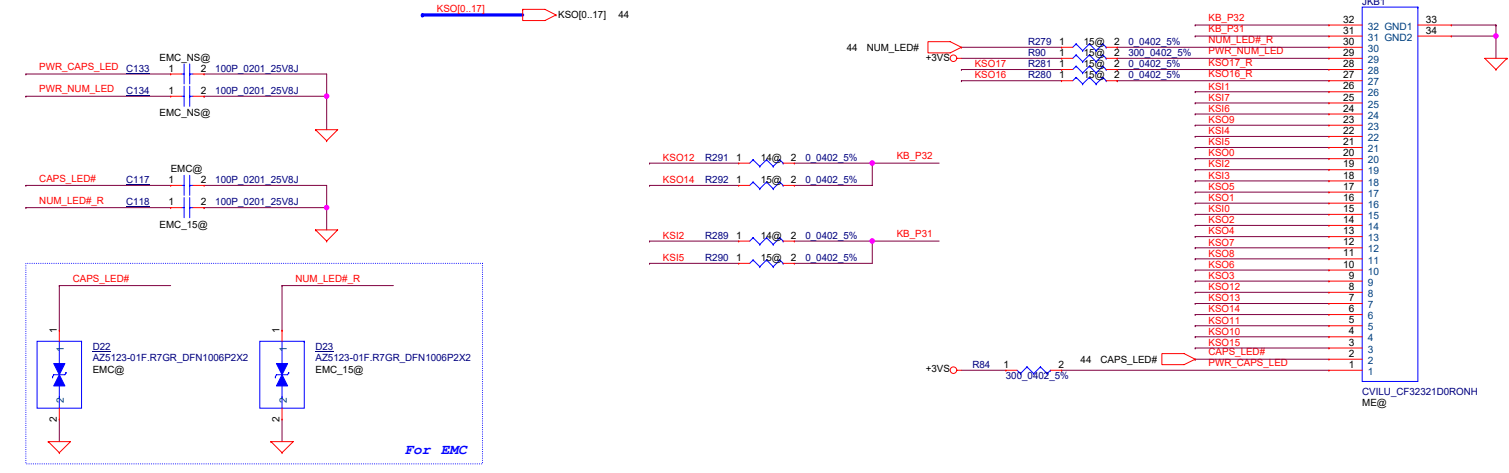
Novo button



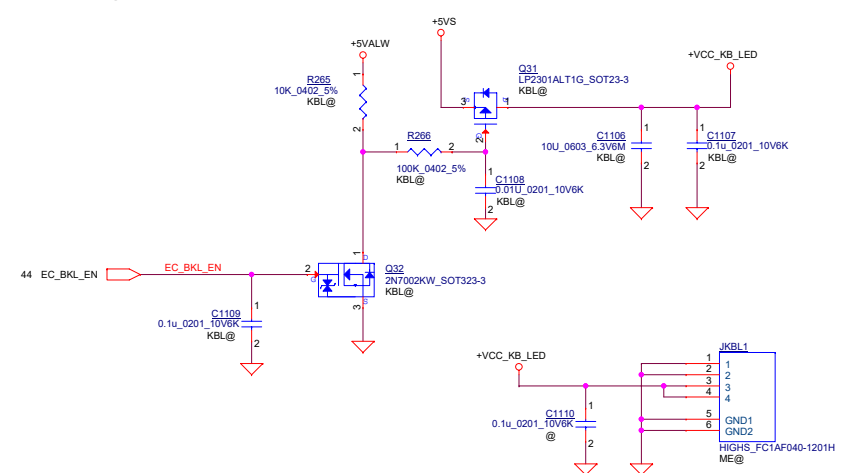
LID switch



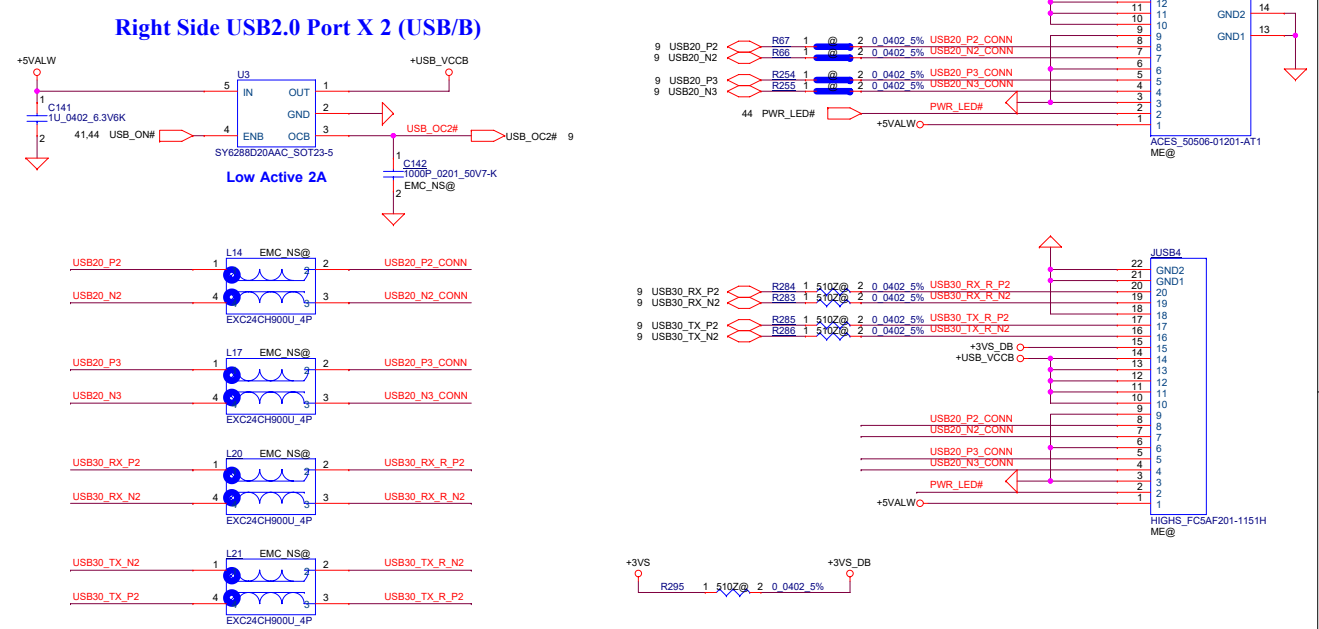
K/B Connector



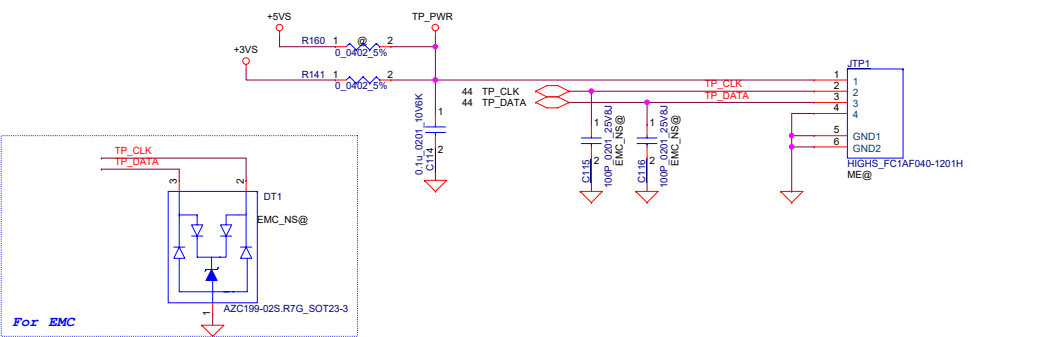
KB Backlight Connector

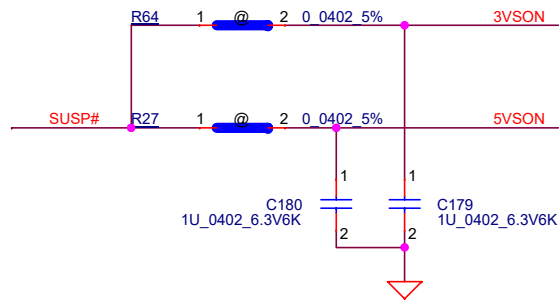


USB DB Connector



TP/B Connector

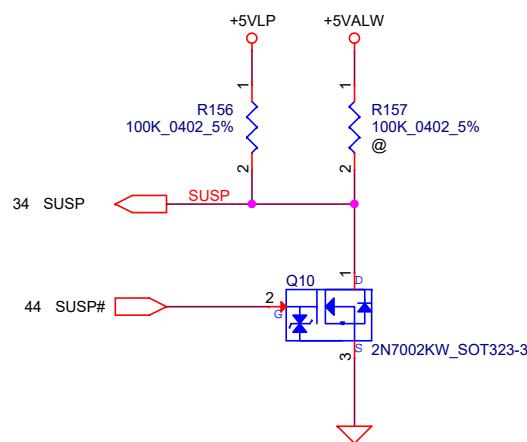
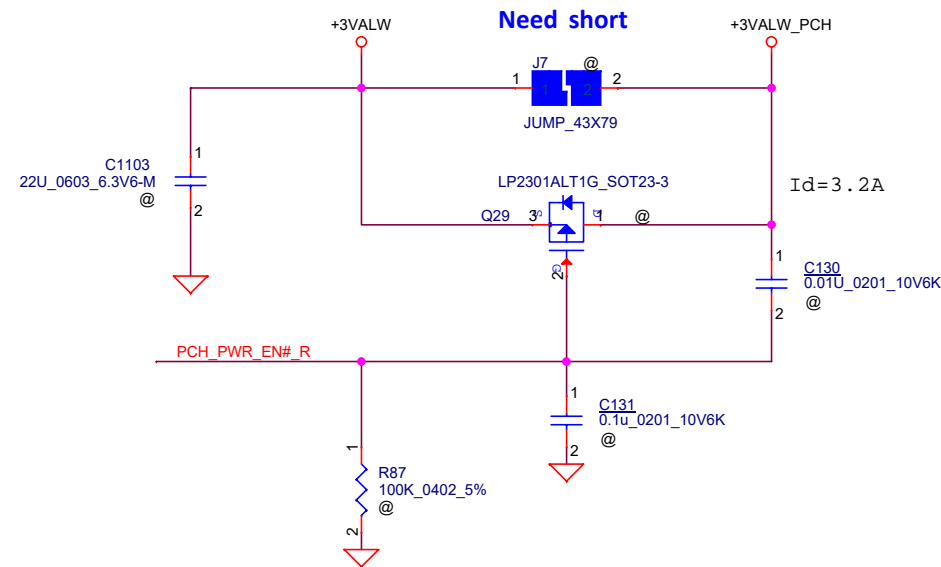
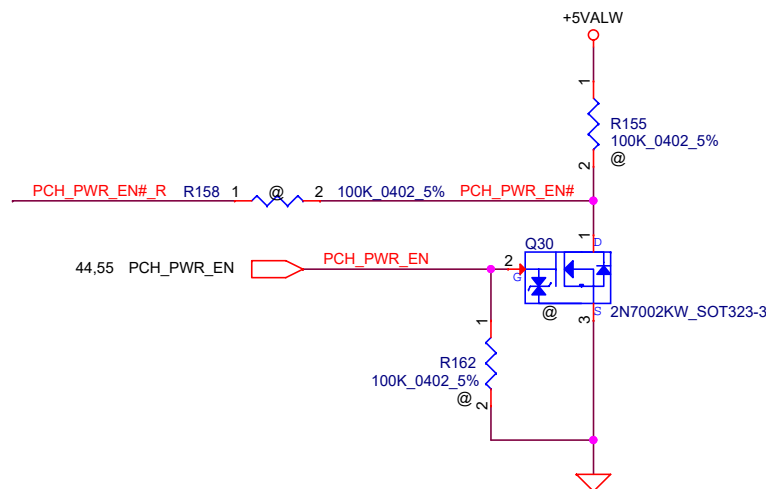
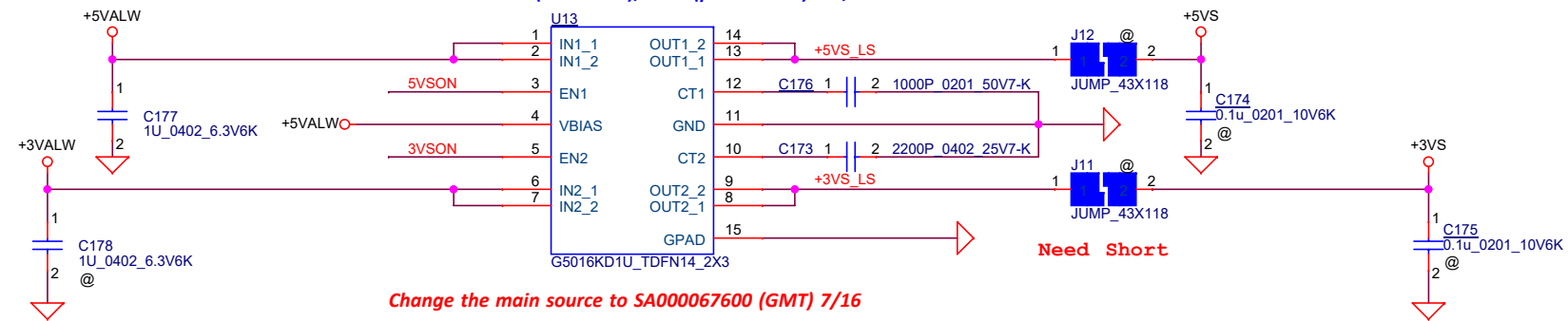




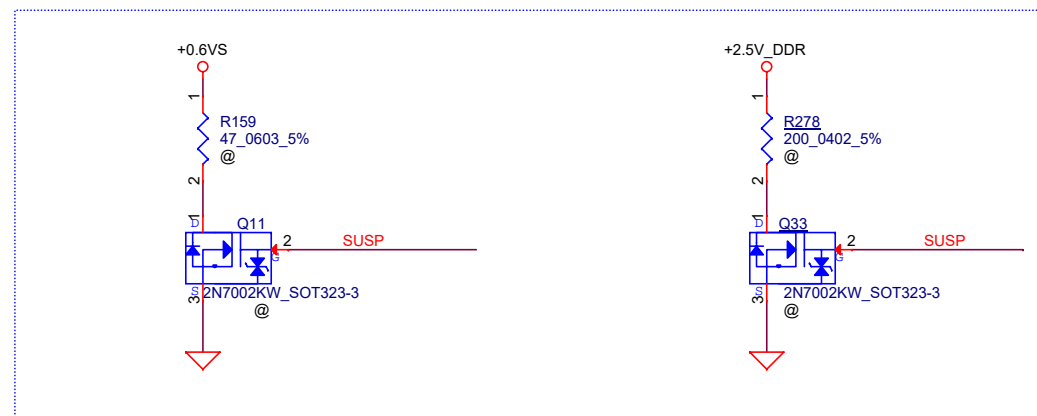
Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms


VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

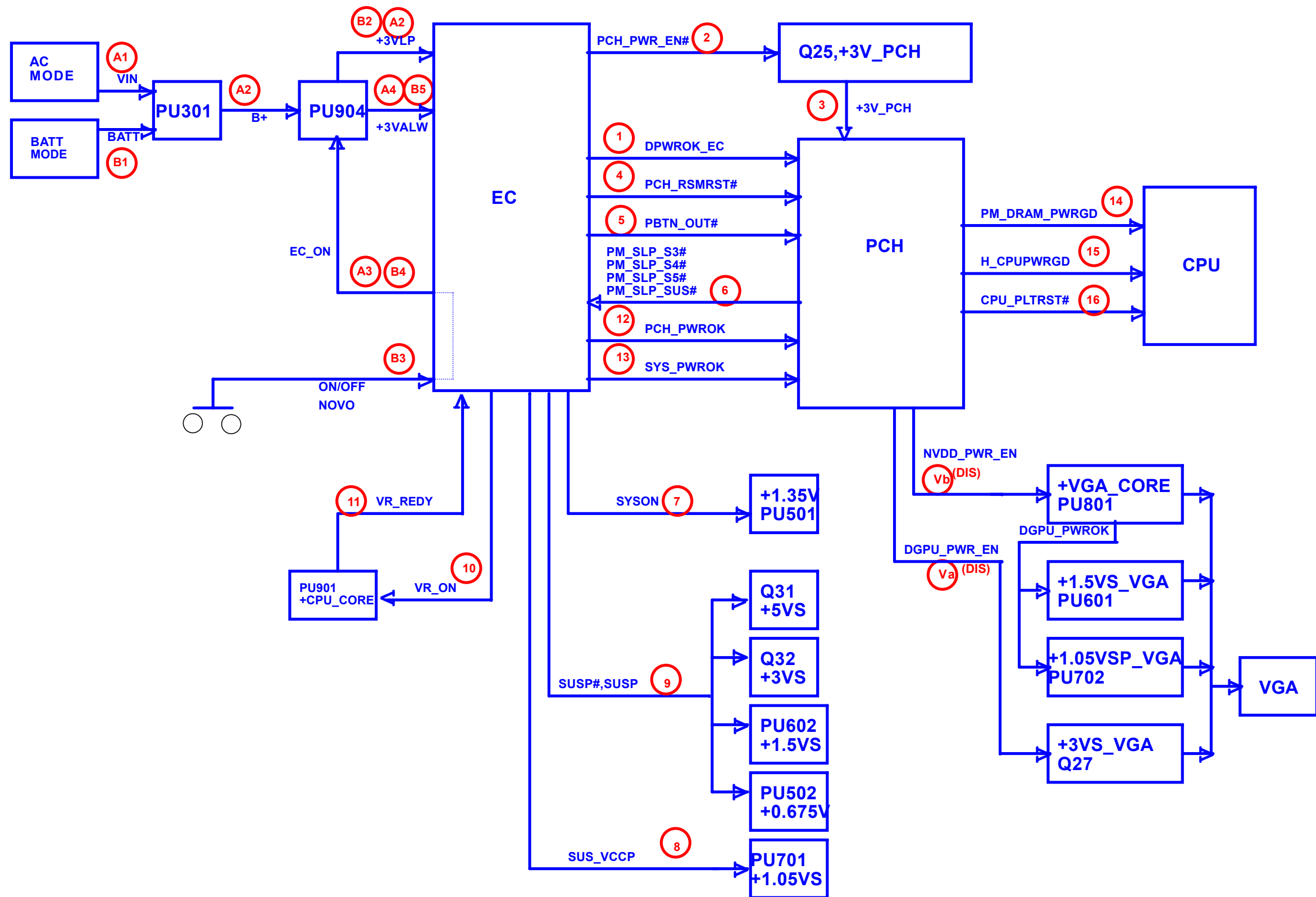


For DisCharge

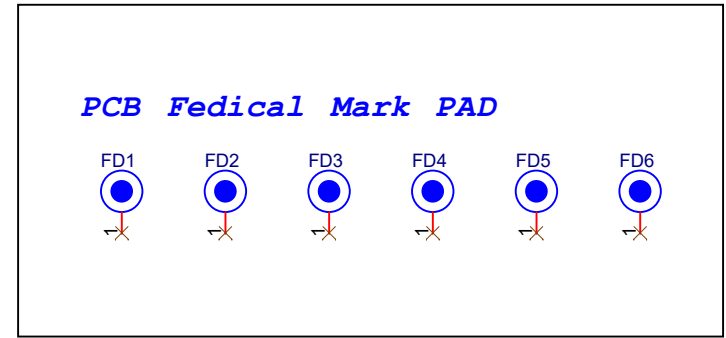



08/29: Need double check enable signal and the resistance

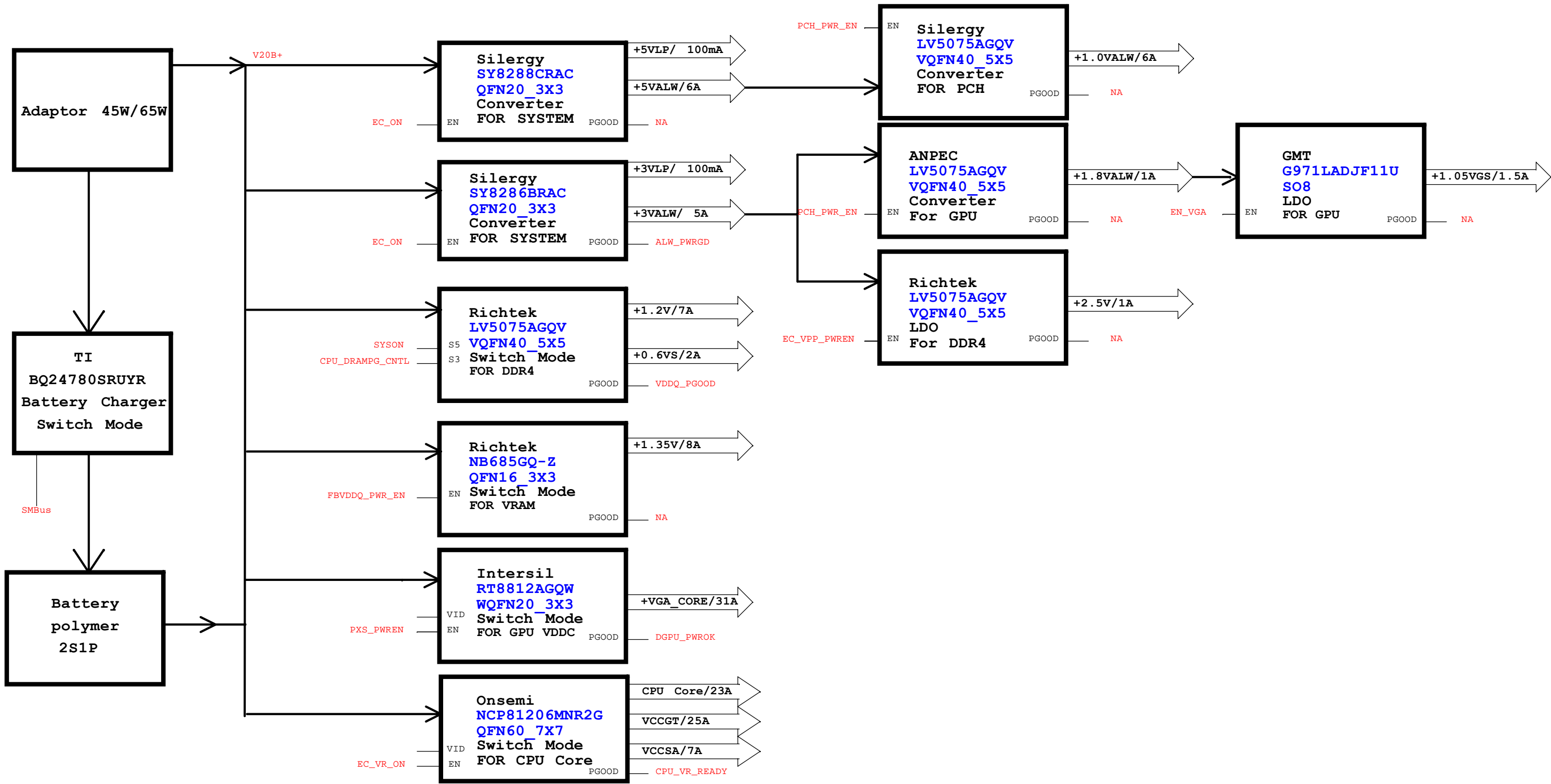
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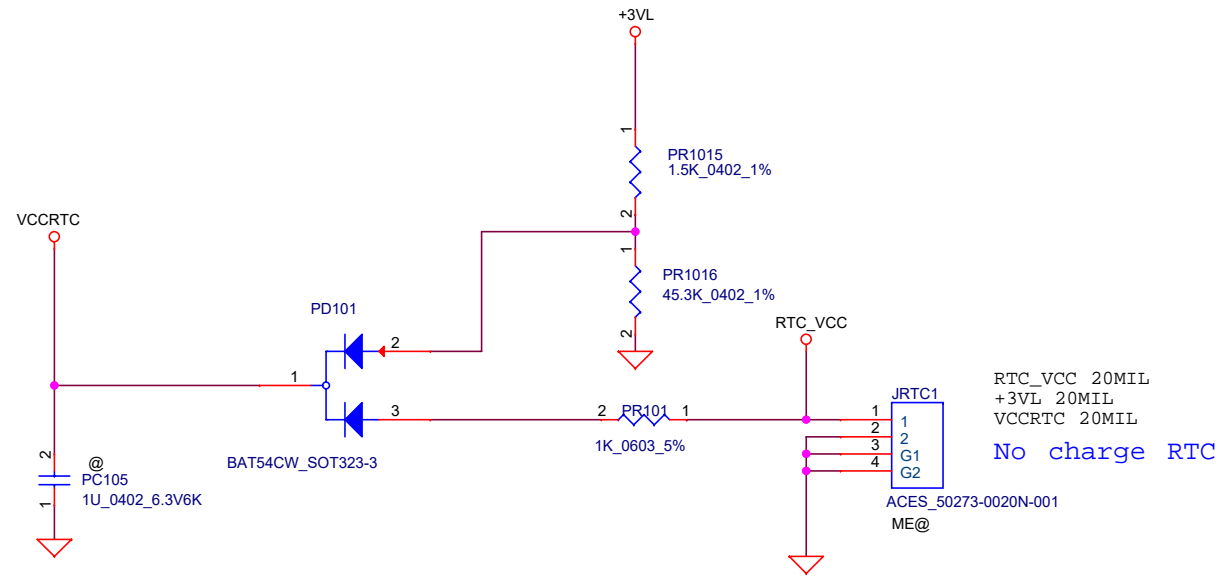
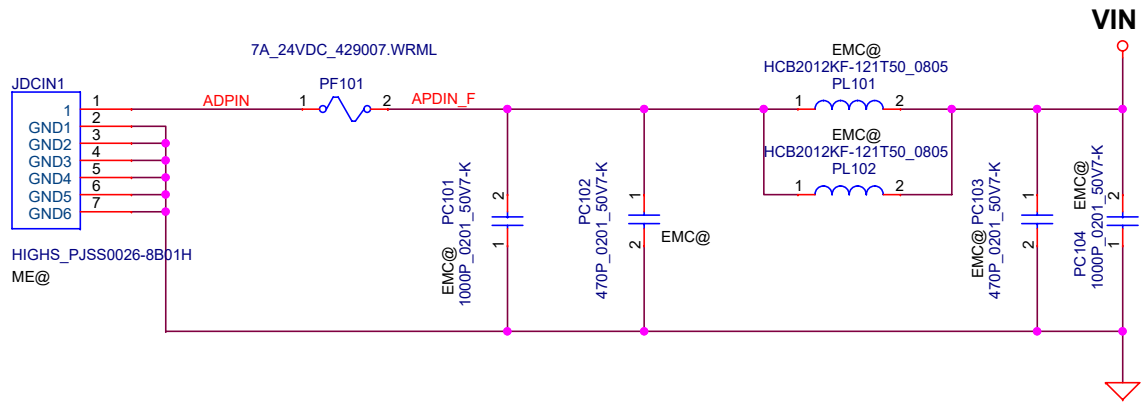


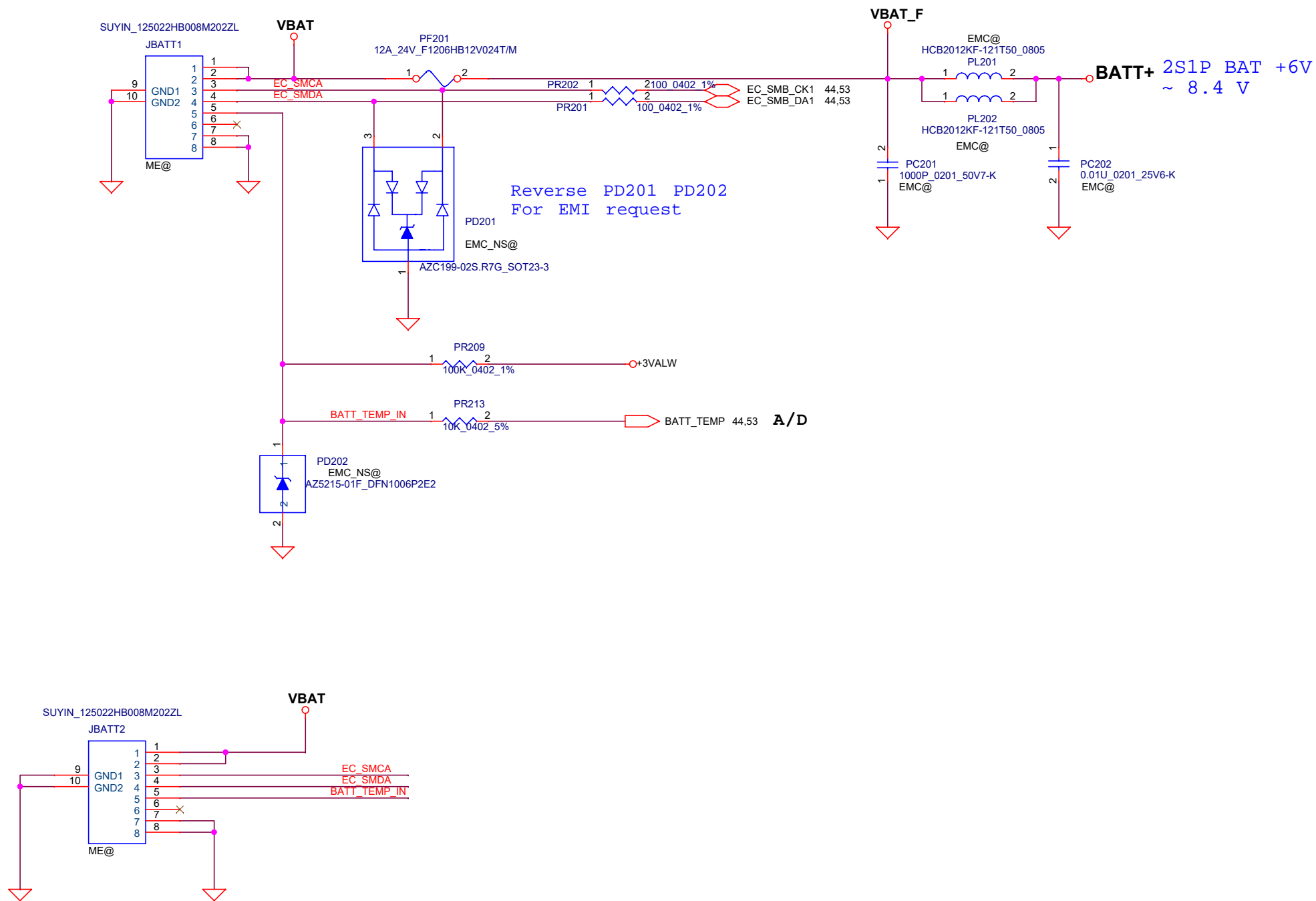
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D								D	
C								C	
B								B	
A								A	

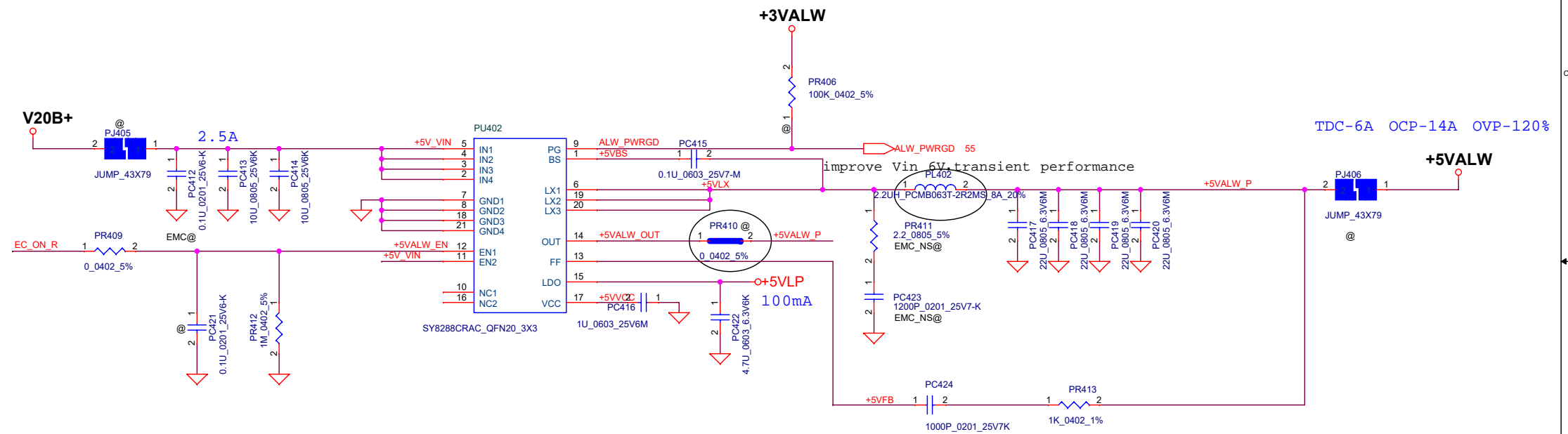
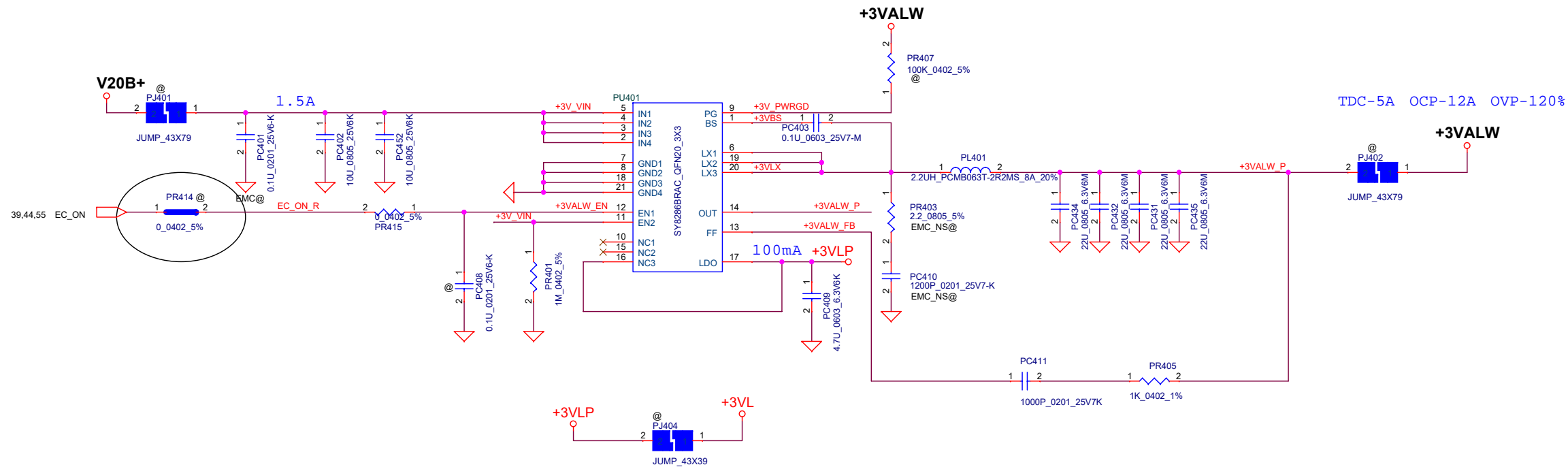


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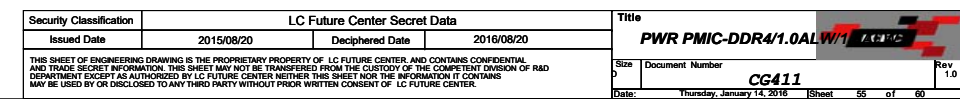




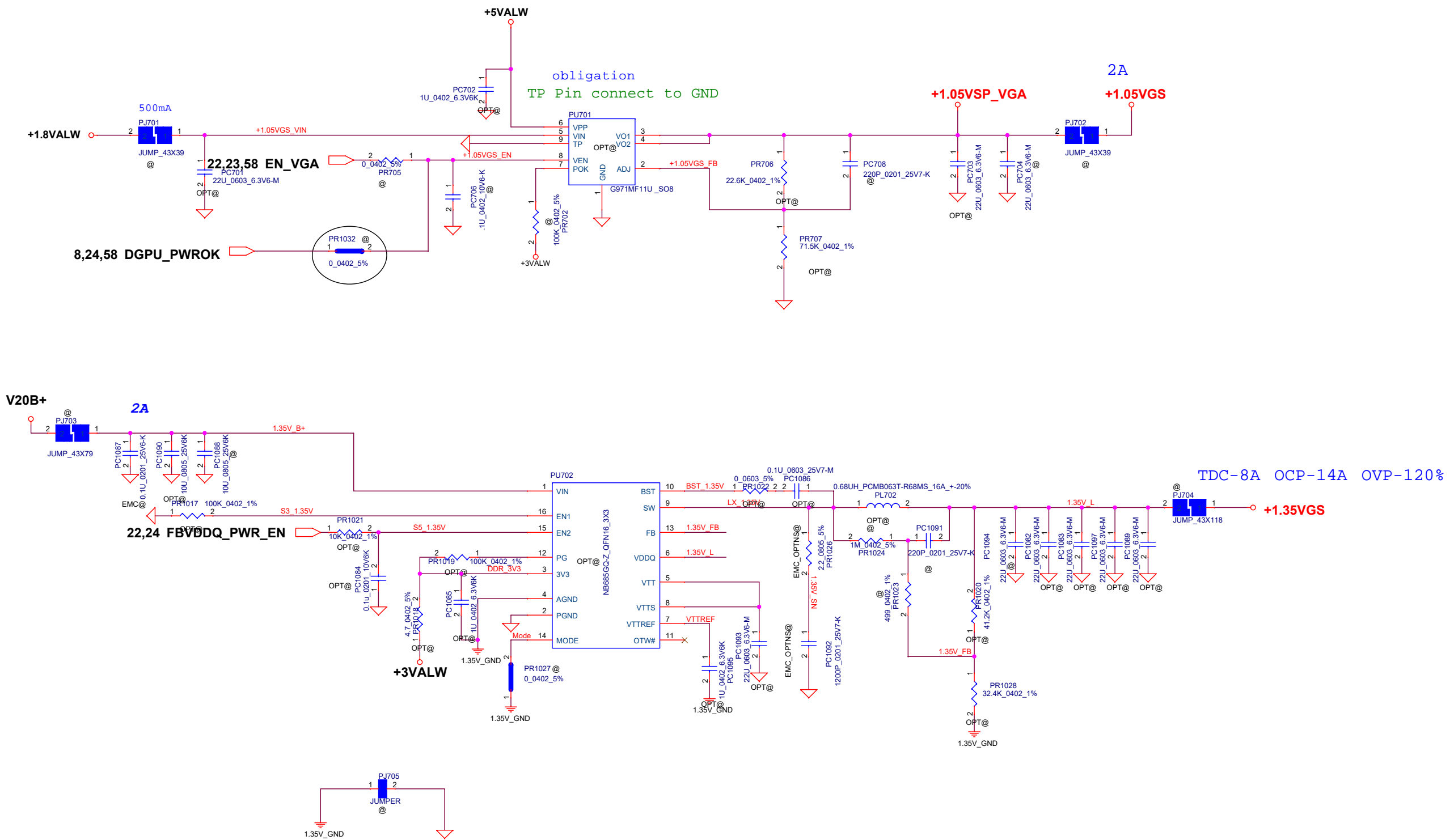







6800pf soft start 2ms
47nf soft start 7ms

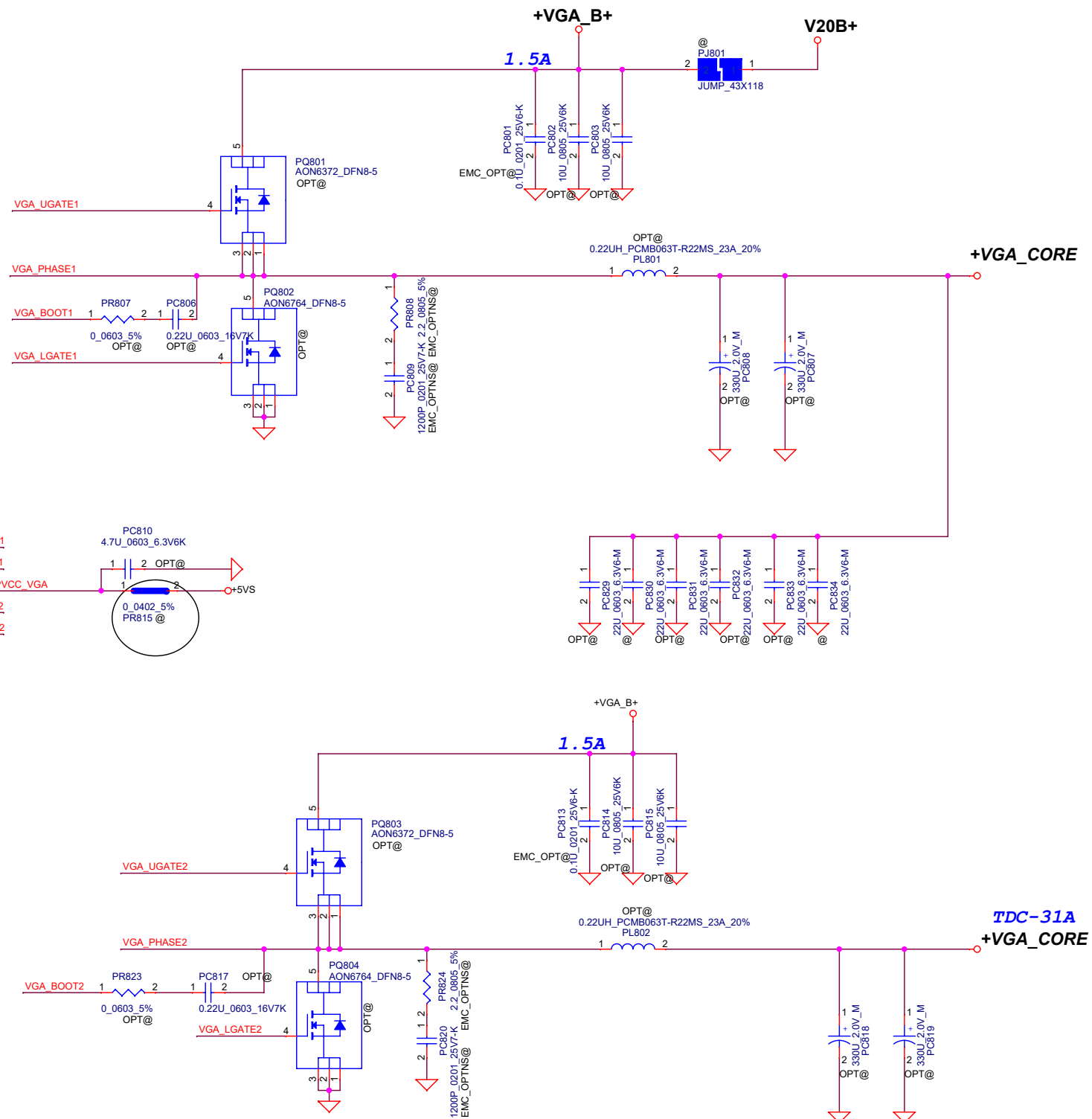
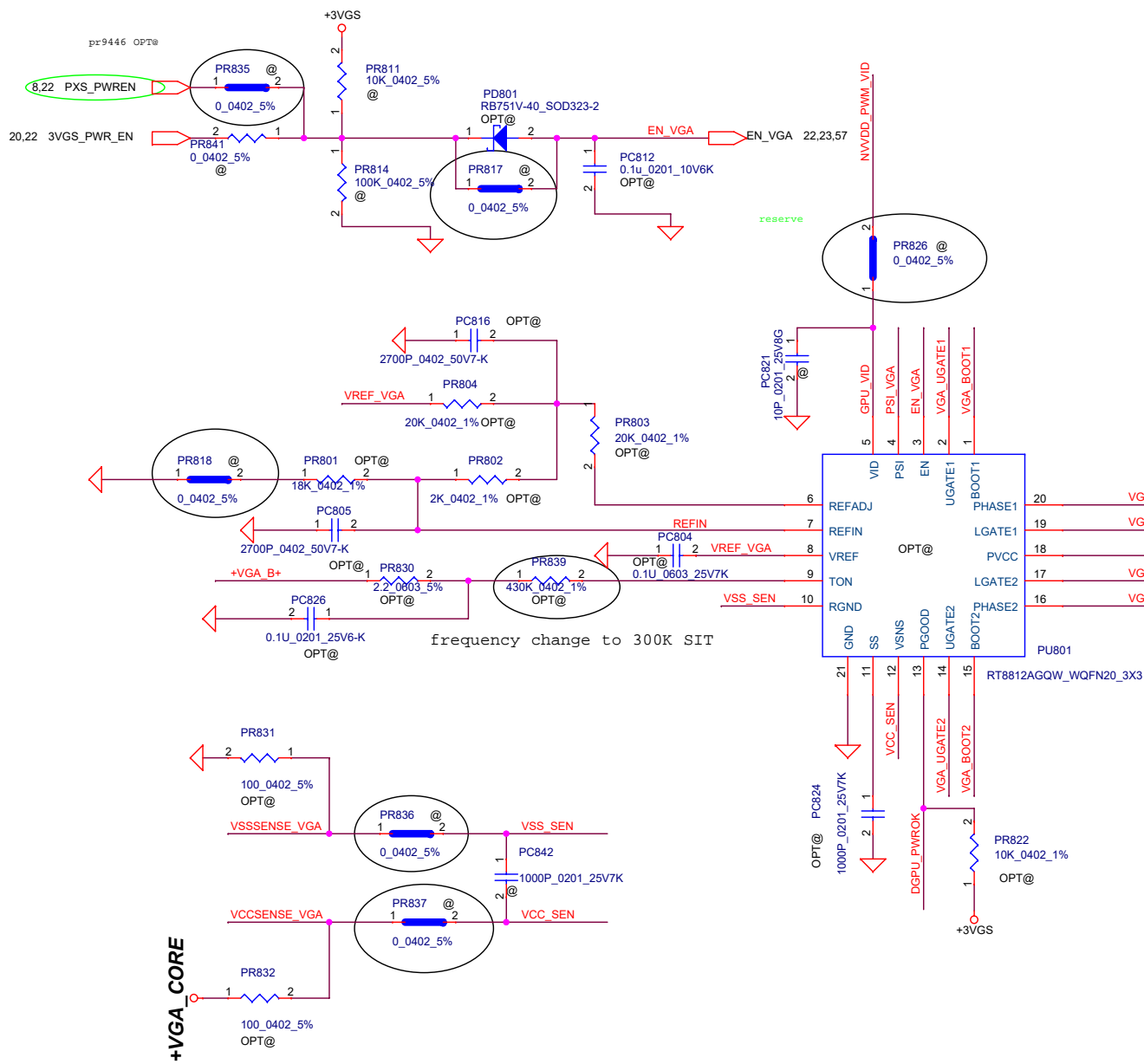
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5		4		3		2		1	
D									
C									
B									
A									



- 20 NVVDD_PWM_VID  NVVDD_PWM_VID
- 20 PSI_VGA  PSI_VGA
- 21 VSSSENSE_VGA  VSSSENSE_VGA
- 21 VCCSENSE_VGA  VCCSENSE_VGA
- 8,24,57 DGPU_PWROK  DGPU_PWROK



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